EXC-1553VME/MCH

EXC-1553VXI/MCH

User's Manual

EXCALIBUR SYSTEMS

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EXC-1553VME/MCH-x
EXC-1553VXI/MCH-x

MULTI-CHANNEL MIL-STD-1553 TEST AND SIMULATION BOARDS FOR VME AND VXI SYSTEMS

GENERAL FEATURES

- UP TO 8 MIL-STD-1553 INDEPENDENT DUAL REDUNDANT CHANNELS
- EASY TO INSTALL AND OPERATE
- 'C' SOFTWARE LIBRARY INCLUDED

RUGGEDIZED, EXTENDED TEMPERATURE RANGE AVAILABLE

- COMPATIBLE WITH VME & VXI SYSTEMS
- "B" AND "C" SIZE CARDS
- 16 BIT DATA TRANSFERS
- SINGLE SUPPLY 5V OPERATION
- VME/VXI COMPLIANCE
  SLAVE: ADDRESS - A16 & A24/A32
  DATA - D16
  INTERRUPT - D08(O), ROAK

FEATURES PER CHANNEL

- OPERATES AS BC, RT, BM, RT CONCURRENT BM
- MULTIPLE PROTOCOL CAPABILITY
  - MIL-STD-1553A
  - MIL-STD-1553B
- AUTONOMOUS OPERATION IN ALL MODES
- 32K WORD MEMORY MAPPED RAM
- 32 CONTROL REGISTERS
- POLLING OR INTERRUPT DRIVEN
- REAL TIME OPERATION
- BUILT IN TEST CAPABILITY

- BC MODE
  - MAJOR / MINOR FRAMES
  - PROGRAMMABLE INTERMESSAGE GAP
  - AUTOMATIC RETRY
- RT MODE
  - SINGLE RT SIMULATION
  - SUBADDRESS DOUBLE BUFFERING
  - CIRCULAR BUFFER MODE
  - MESSAGE ILLEGALIZATION
  - 16 BIT TIME TAG
  - PROGRAMMABLE BROADCAST MODE
- BM MODE
  - 16 BIT TIME TAG
  - FILTERING PER RT
  - INTERRUPT HISTORY LIST
  - PROGRAMMABLE MONITOR BLOCK COUNT

The EXC-1553VME/MCH-x and EXC-1553VXI/MCH-x are multi-channel (up to 8) Mil-Std-1553 interface cards for VME and VXI systems. Each channel is Dual Redundant and supports both 1553A and 1553B protocols. Each channel provides Bus Controller, Remote Terminal, Bus Monitor, and Remote Terminal Concurrent Bus Monitor operation. The user controls the operation of each channel by accessing dedicated memory-mapped control registers and 32Kx16 RAM.

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1.0 INTRODUCTION

The EXC-1553VME/MCH-x and the EXC-1553VXI/MCH-x family of products provide a multi-channel Mil-Std-1553 test and simulation environment on VME and VXI systems. The name "EXC-1553VME/MCH" will be used as a generic name throughout this manual and denotes both boards. Based on the latest ASIC technology (UTMC "SìMMIT™-XT" 1553 protocol controller) which substantially reduces the area required per channel, the EXC-1553VME/MCH provides a very powerful and flexible test environment capable of handling the most sophisticated applications. The EXC-1553VME/MCH enables the user to design the test/simulation environment in a modular manner while providing complete flexibility in choosing the data processing power required.

The EXC-1553VME/MCH provides Bus Controller, Remote Terminal, Bus Monitor, Remote Terminal Concurrent Bus Monitor operation on each channel enabling Concurrent operation on multiple independant Mil-Std-1553 dual redundant buses. As card operation is set by parameters stored in Ram, test setups may be altered in real time, as dictated by the application.

For harsh environments (in flight) applications the EXC-1553VME/MCH is available in a ruggedized, extended temperature (-40° to +85° C) version. See Ordering Information for specifying available options.

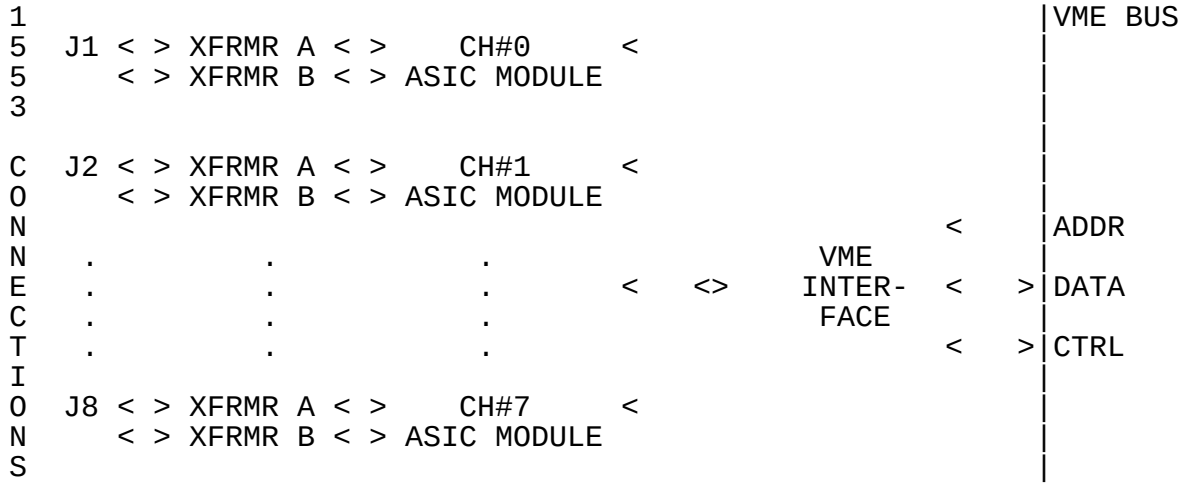


Figure 1. EXC-1553VME/MCH-x Block Diagram

2.0 INSTALLATION & CONNECTIONS

Before installing the card it is very important to determine which 64 byte section of A16 address space is available for the cards VME/VXI Configuration Registers. When this is determined, the SW1 dipswitch should be set accordingly (see Dip Switch Settings section). The user should also decide if A24 or A32 address space is to be used and set the appropriate jumper, JP33 (see Jumpers section).

1553 devices may be connected to the 1553 bus either directly (Direct Coupled) or via a bus coupling stub (Transformer Coupled). Jumpers JP1 to JP32 must be set to inform the card which coupling method is being used for each bus the card is connected to (see Jumpers section).

2.1 1553 Bus Connections

For short distances, direct coupling may be used to connect the EXC-1553VME/MCH directly to another 1553 device. The user must make certain that the cable connecting the two devices is properly terminated with 78 ohm resistors to insure data integrity. Figure 2a shows how two 1553 devices may be connected in Direct mode.

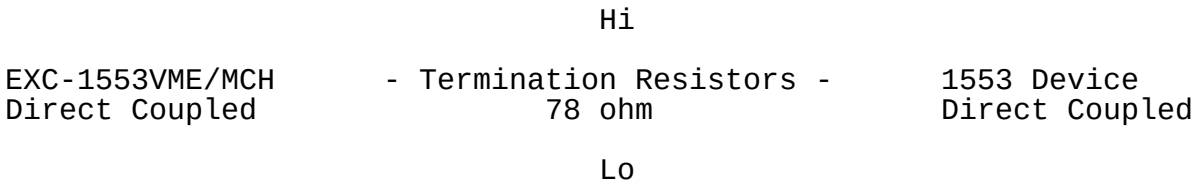


Figure 2a. Direct Coupled Connection (One Bus Shown)

For users wishing to operate in the more standard Transformer Coupling mode, stub coupler devices are available from a number of manufacturers. North Hills Electronics, Inc. supplies a three stub coupler (PN# DB30010) as well as 78 ohm terminators (PN# RT500078). Two terminators are required for each coupler which services a single bus (e.g. BUS A). Figure 2b shows how 1553 devices may be connected in Transformer (Stub) mode.

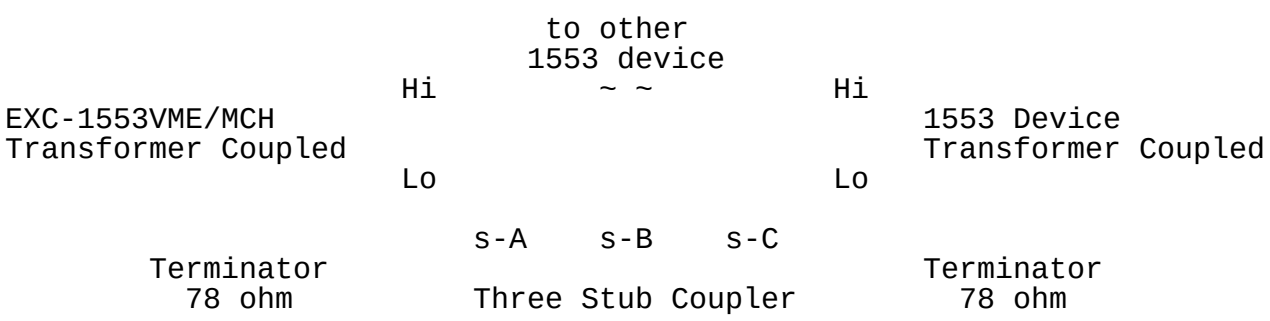


Figure 2b. Transformer Coupled Connection (One Bus Shown)

3.0 VME/VXI INTERFACE

The EXC-1553VME/MCH complies with the following VME/VXI parameters:

VME parameters

Board type - SLAVE
Addressing - A16 and A24/A32
Data - D16
Interrupts - IRQ1-7*; D08(O); ROAK

VXI parameters

Device Class - Register Based
Manufacturer ID - 3924dec (F54H)
Address Space - A16/A24 or A16/A32
Required Memory - 512K; m=0100(A24)/1100(A32)
Model Code - 1363dec (553H)

The board interfaces to the VME via a 16-bit data bus. Note that all accesses to the card must be 'Word' accesses (16 bits). All byte accesses will be ignored. The board may be accessed by using addresses in the form:

For accessing VME/VXI Configuration registers:

XXXX (H) (A16 mode) with ADDRESS MODIFIER CODES: 29, 2D

For accessing Data Storage Area and Control Registers:

XX XXXX (H) (A24 mode) with ADDRESS MODIFIER CODES: 39, 3A, 3D, 3E
or
XXXX XXXX (H) (A32 mode) with ADDRESS MODIFIER CODES: 09, 0A, 0D, 0E

The memory map is divided into two distinct blocks:

1. VME/VXI Configuration Registers.
2. 1553 Message Storage Area and Control Registers.

The VME/VXI Configuration Registers are used for setting up the board within the user's VME or VXI system. The 1553 Message Storage Area and Control Registers are used to control the operation of the board on the 1553 bus.

3.1 VME/VXI Configuration Registers

The VME/VXI Configuration registers are located within a 64 byte block in the A16 address space between the addresses 49152 (dec) [C000H] and 65472(dec) [FFC0H]. The base address of the Configuration registers is determined by the following equation:

Base Address (dec.) = V*64 + 49152 (dec.)

V, the "Logical Address" of the card, is an integer which varies between 0 and 255 and is defined by the user via the 8 pole dipswitch SW1 (see Dip Switch Settings section). In order to ensure correct operation of the board within the user's VME or VXI system the Configuration registers must be (re)initialized after power up or after assertion of SYSRESET*. For a full explanation of the VXI Configuration registers and other topics relating to operation of the VXI bus refer to the "VXI Bus System Specification".

3.1.1 Configuration Register Memory Map

PROGRAMMABLE TIMER CLOCK REG.	BASE + 30 (H)
VECTOR#7 REGISTER	BASE + 2E (H)
VECTOR#6 REGISTER	BASE + 2C (H)
VECTOR#5 REGISTER	BASE + 2A (H)
VECTOR#4 REGISTER	BASE + 28 (H)
VECTOR#3 REGISTER	BASE + 26 (H)
VECTOR#2 REGISTER	BASE + 24 (H)
VECTOR#1 REGISTER	BASE + 22 (H)
VECTOR#0 REGISTER	BASE + 20 (H)
OFFSET REGISTER	BASE + 06 (H)
STATUS/CONTROL REGISTER	BASE + 04 (H)
DEVICE TYPE REGISTER	BASE + 02 (H)
ID REGISTER	BASE + 00 (H)

Figure 3. Configuration Registers Map

3.1.2 ID Register (VXI only) BASE + 00 READ ONLY

The contents of this 16-bit register provides the following information about the board's configuration.

```
          0   1     A32 ADDRESS SPACE   (JP33 not installed)

          0   0     A24 ADDRESS SPACE   (JP33 installed)

 15  14  13  12  11  10   9   8   7   6   5   4   3   2   1   0

  1   1           1   1   1   1   0   1   0   1   0   1   0   0
```

DEVICE CLASS: REGISTER BASED

MANUFACTURER ID: F54 (Hex) 3924 (Dec.)

Note: This register contains the same value whether set up for VME or VXI installation. The VXI specification requires all VXI devices to identify themselves via an ID register. This location is not defined under the VME specification.

3.1.3 Device Type Register (VXI only) BASE + 02 READ ONLY

This 16 bit register contains a fixed Device Type Identifier as well as a four bit field which reflects the Required Memory usage of the card.

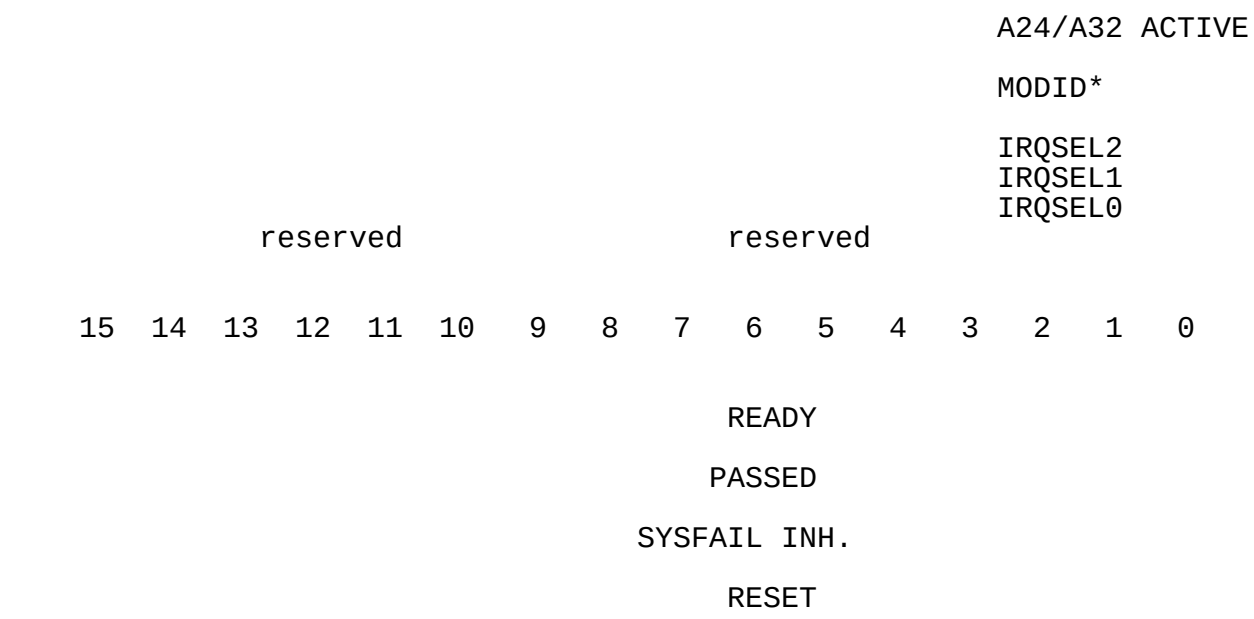
```
  1   1   0   0   REQUIRED MEMORY (m) - A32 SPACE   (JP33 not installed)

  0   1   0   0   REQUIRED MEMORY (m) - A24 SPACE   (JP33 installed)

 15  14  13  12  11  10   9   8   7   6   5   4   3   2   1   0

                  0   1   0   1   0   1   0   1   0   0   1   1
```

MODEL CODE: 553 (Hex) 1363 (Dec)

Note: This register contains the same value whether set up for VME or VXI installation. The VXI specifications requires the user to let the system know how much memory the device requires. This is known as the 'm' value in VXI parlance. This location is not defined under the VME specification.

3.1.4 Status Register (VXI & VME) BASE + 04 READ ONLY

A read of this 16 bit register provides information as defined below.

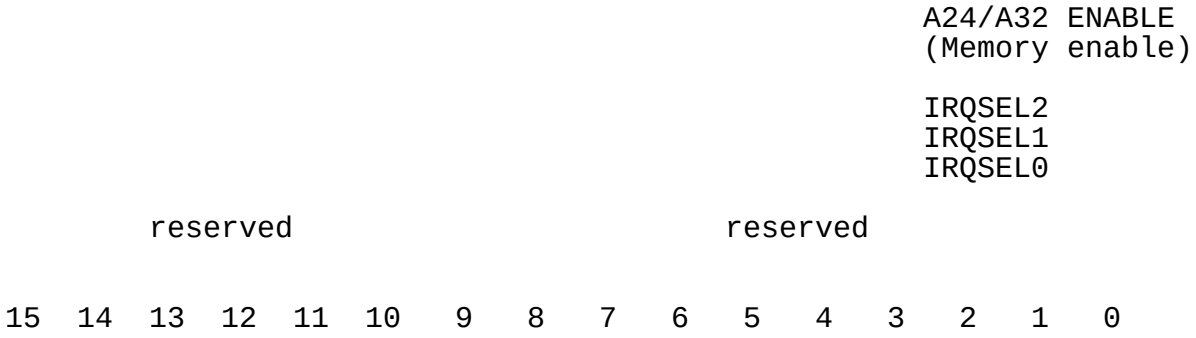


Note: The MODID, READY, PASSED, SYSFAIL INHIBIT and RESET functions are included to maintain compliance with the VXI specification. It is recommended that VME users make use of the software reset described in the main body of this manual.

Bit_Name	Description
RESET	Indicates the state of the RESET bit in the Control Register
SYSFAIL INHIBIT	Indicates the state of the SYSFAIL INHIBIT bit in the Control Register
PASSED	This bit is always set to "1"
READY	A "1" indicates that the power up sequence has completed and that the card is ready to accept commands. This bit is a logical 'AND' of all installed channels's READY bit.
IRQSEL 2-0	Indicates the state of the IRQSEL2-0 bits in the Control Register
MODID*	Indicates the inverted value of the VXI bus "MODID" line.
A24/A32 ACTIVE	Indicates the state of the A24/A32 ENABLE bit in the Control Register

3.1.5 Control Register (VXI & VME) BASE + 04 WRITE ONLY

Writing to this 16-bit register causes the actions listed below to be executed by the card. Note that all bits in this register are set to "0" after assertion of VME bus line SYSRESET*.



Bit_Name	Description
RESET	Writing a "1" to this bit forces the card into the "RESET" state. The user must not write a "0" into this bit for at least 100 usec after writing a "1" into it. That is, once in the "RESET" state, the card must remain in this state for at least 100 usec. While in the "RESET" state the card is completely inactive and will not respond to any commands. Upon releasing the card from the "RESET" state (write "0" to this bit), the card will perform its self test routines. The board may also be reset via the Software Reset Registers defined within the main body of this manual. This second method is the preferred mechanism for resetting the card.
SYSFAIL INHIBIT	This bit has no effect.
IRQSEL 2-0	Writing to these bits selects which one of the VME bus Interrupt Request lines IRQ1* -- IRQ7* will be driven active when the card generates an interrupt. Refer to section "Using Interrupts on VME" in following. The following table shows the relationship between IRQSEL 2-0 and IRQ7-1.

SELECTED IRQ LINE	**IRQSEL2**	**IRQSEL1**	**IRQSEL0**
NONE	0	0	0
IRQ1*	0	0	1
IRQ2*	0	1	0
IRQ3*	0	1	1
IRQ4*	1	0	0
IRQ5*	1	0	1
IRQ6*	1	1	0
IRQ7*	1	1	1

Bit_Name	Description
A24/A32 ENABLE (Memory Enable) 1553	Writing a "1" to this bit enables access to the card's Message Storage Area and Control Registers residing in A24 or A32 VME address space. If this bit is set to "0" none of the on card registers and memory which are resident in the A24 or A32 address space may be accessed. The Configuration registers, of course remain accessible regardless of the state of this bit, as they reside in the A16 address space of the card.

3.1.6 Using Interrupts on VME

The Interrupt generated on the selected IRQ* line is the "logical OR" of all interrupt generating sources on the card. An interrupt which was generated by Channel #0 will result in the interrupt routine whose vector resides in VECTOR#0 register to be executed. The card will place the value in the VECTOR#0 register, called the STATUS/ID, onto the VME data lines when issuing the interrupt acknowledge cycle. The user's processor will use this value to determine which entry in the user's interrupt vector table to jump to. Within this interrupt routine the actual source of the interrupt can be determined by polling the Pending Interrupt Register. Likewise, an interrupt which was generated by Channel #n will result in the interrupt routine whose vector resides in VECTOR#n register to be executed.

If case of multiple pending interrupt requests, the highest priority request STATUS/ID will appear first. After the user services this interrupt, a second interrupt will be generated for the next pending interrupt. The priorities are defined as follows:

Request name	**Priority**
Channel#0 Request	Highest
Channel#1 Request	
Channel#2 Request	
Channel#3 Request	
Channel#4 Request	
Channel#5 Request	
Channel#6 Request	
Channel#7 Request	Lowest

For all interrupts, the serviced interrupt request is cleared automatically at the end of the interrupt acknowledge cycle. This method is referred to within the VME specification as ROAK (Release on AcKnowledge).

3.1.7 Offset Register (VXI & VME) BASE + 06 Read/Write

This 16 bit read/write register defines the base address of the card's A24 or A32 memory and registers. If A24 addressing is used the 5 most significant bits of the Offset register are the values of the 5 most significant bits of the card's memory and register addresses and the 8 least significant bits of the register are not used. If A32 addressing is used the Offset register represents the 13 most significant bits of the card's memory and register addresses. Thus, the Offset register bits 15 through 11 map to the address lines A23 through A19 for the A24 Address Space, and the Offset register bits 15 trough 3 map to address lines A31 through A19 for the A32 Address Space.

A24 ADDRESSING EXAMPLE: required base address = 18 0000 H;
write 18XX H to Offset register

OFFSET

X = don't care

0	0	0	1	1	X	X	X	X	X	X	X	X	X	X	X
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A23	A22	A21	A20	A19											

A32 ADDRESSING EXAMPLE: required base address = FF38 0000 H;
write FF38 H to Offset register

OFFSET

1	1	1	1	1	1	1	1	0	0	1	1	1	X	X	X
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A31	A30	A29	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19			

3.1.8 Vector#n Register (VXI & VME) BASE + 20(H) + 2n Read/Write

In the case of an interrupt generated by Channel #n, the 8 least significant bits of this 16 bit register, known as the STATUS/ID, are used as the interrupt vector during the ensuing interrupt acknowledge cycle. The card is a D08(O) INTERRUPTER, and as a result will place these 8 bits on lines D00-D07 of the VME bus during the interrupt acknowledge cycle. Refer to section "Using Interrupts on VME". The 8 most significant bits of this register are don't care.

X	X	X	X	X	X	X	X	STATUS/ID							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

X = don't care

3.1.9 Programmable Timer Clock Register (VXI & VME) BASE + 30(H) Read/Write

This register selects the programmable timers clock value for the channel timers. Each channel can be individually programmed to use an internal fixed clock or to use this programmable clock (see PTCE bit within channel's Control Register). This clock is derived from the VME SYSCLK signal (16MHz). There are two reasons to use the programmable clock. First, a desired timer resolution different from the fixed one (64 usec). Second, a request for the timers synchronization to the VME clock and/or synchronization to other boards residing in the VME system. Only the least significant 8 bits are used. Writing a value of 0 to this register will stop the programmable timer clock. The highest possible clock resolution that can be achieved is 0.25 usec (4MHz). The lowest possible resolution is 32 usec (31.250KHz).

X	X	X	X	X	X	X	X	Timer Clock Value							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

X = don't care

The formula for calculating the Timer Clock Value (TCV) is:

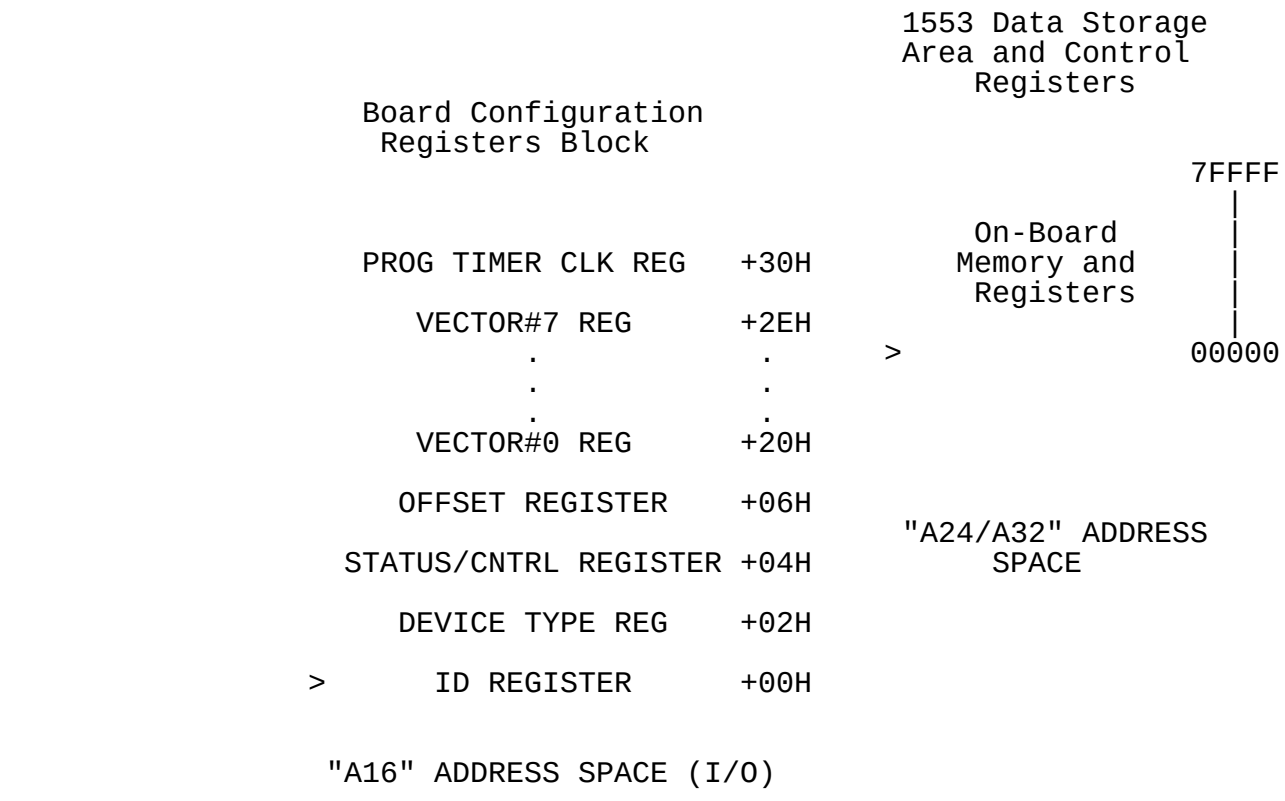
$$TCV = \frac{16{,}000{,}000}{2 \times freq(Hz)} - 1$$

Example: Desired Programmable Timer Clock frequency is 31.250KHz (= 32 usec resolution)

$$TCV = \frac{16{,}000{,}000}{2 \times 31250} - 1 = 256 - 1 = 255 \text{ Dec (FFH)}$$

Write "00FFH" to this register

3.1.10 Memory/Registers Address Mapping Diagram



.
Logical Address
Dip Switch; SW1

Figure 4. Memory/Registers Address Mapping Diagram

A16 ADDRESSING EXAMPLE:

Given:
Required configuration registers base address = E000(H)

Then:
Set dip-switch SW1 to LOGICAL ADDRESS = 80(H)

	OFF	ON	ON	ON	ON	ON	ON	ON
SW1	1	2	3	4	5	6	7	8

4.0 GENERAL MEMORY MAP

The board occupies 512Kx8 of the VME A24 or A32 address space, which are mapped via the Offset Register within the VME/VXI Configuration Registers. The 256K words of memory space occupied by the EXC-1553VME/MCH is divided into eight blocks of 32K words, one for each channel.

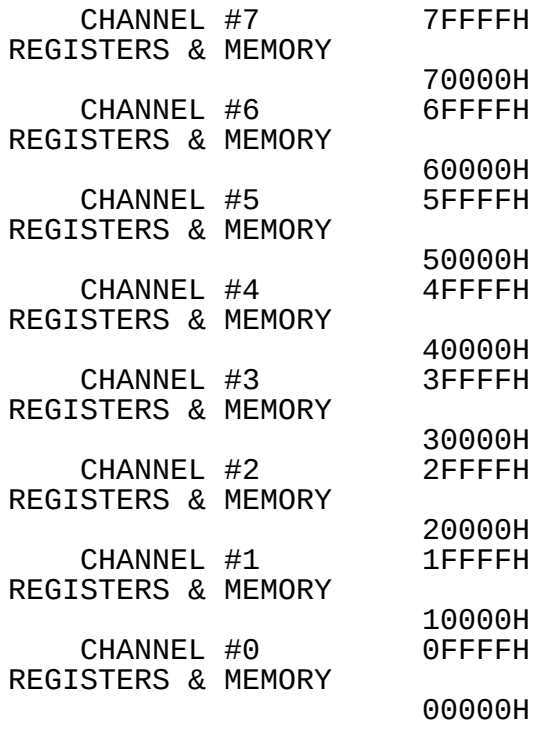


Figure 5. EXC-1553VME/MCH Memory Map

Note: In case of a partially occupied board, ignore the memory locations related to the non-occupied channels.

5.0 CHANNEL GENERAL OPERATION

The description of operation of the EXC-1553VME/MCH, which follows, applies to each available 1553 channel.

Each channel occupies a 32K words area of the board's Memory Address Space. This area is shared between the Channel Memory Block, used for data and message control, Channel Register Block, used for various control registers, and the Channel Reset Register, used for channel software reset (see figure 6). A powerful RISC processing unit (UTMC "SìMMIT™-XT" 1553 protocol controller) provides automatic message handling, message status, general operational status and interrupt information. The user has direct access to all control registers and data blocks in Real Time. The user controls the operation of the card by accessing the Ram and control registers. The EXC-1553VME/MCH may be configured to support Mil-Std-1553B as well as Mil-Std-1553A protocol.

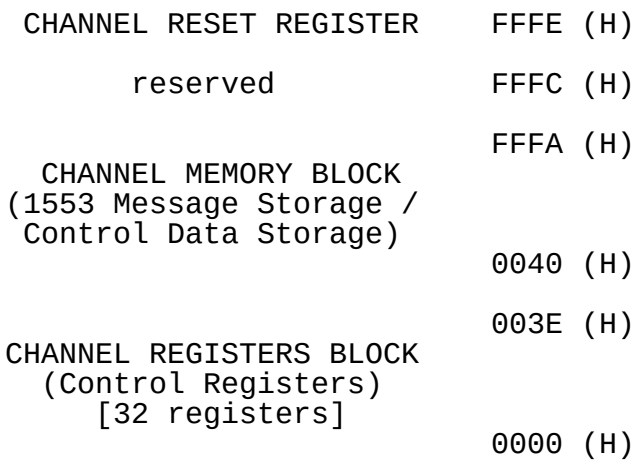


Figure 6. Channel Memory Map

5.1 Channel Reset Register FFFE (H)

Writing to this register (data = don't care) performs a software reset of the channel. The channel will act as if POWER had been switched off then on; encoder, decoder, all control registers, and associated logic will be reset. Note that assertion of reset terminates immediately command processing. The reset operation takes 5 usec to execute.

5.2 Reserved FFFC (H)

This location is reserved.

6.0 OPERATIONAL MODES

The following describes the operation of a single channel of the EXC-1553VME/MCH in each of its operational modes. Note that the operation and addressing of the next channels is identical to that of the first with the appropriate base address.

6.1 BUS CONTROLLER MODE (BC MODE)

6.1.1 Control Registers For BC Mode

The control registers are read/write unless otherwise stated. All control registers **must** be accessed in word mode. All control register bits are active high and are reset to '0' unless otherwise stated.

reserved	003E (H)
	0012 (H)
COMMAND BLOCK POINTER REG	0010 (H)
MINOR FRAME TIMER	000E (H)
BIT WORD REG	000C (H)
INT LOG LIST POINTER REG	000A (H)
PENDING INTERRUPT REG	0008 (H)
INTERRUPT MASK REG	0006 (H)
CURRENT COMMAND BLOCK REG	0004 (H)
OPERATIONAL STATUS REG	0002 (H)
CONTROL REGISTER	0000 (H)

Figure 7. BC Control Registers Map

6.1.1.0 Description Of BC Mode Control Registers

6.1.1.1 Control Register 0000 (H) Read/Write

The Control Register's function is to configure the EXC-1553VME/MCH for operation. To make changes to the BC and this register, the STEX bit (Bit 15) must be logic zero. To operate the EXC-1553VME/MCH as a bus controller, use the following bits.

Bit	Name	Description
15	STEX	Start Channel Execution. Assertion of this bit commences operation of the EXC-1553VME/MCH channel. A Control Register write negating this bit inhibits operation of the channel. After execution begins, a write of logic zero will halt the EXC-1553VME/MCH channel after completing the current 1553 message.
14	SBIT	Start Channel B.I.T. Assertion of this bit places the channel into the Built-In Test routine. The BIT test takes 1 ms to execute and has a fault coverage of 93.4%. Once the channel has been started, the host must halt the channel in order to place the channel into the Built-In Test routine (STEX = 0). Note: If Start BIT (SBIT) and Start Execution (STEX) are both set on one register write, BIT has priority.
13-11	reserved	Should be set to '0'.
10	PTCE	Programmable Timer Clock Enable. Assertion of this bit enables a programmable clock used with an internal counter for variable minor frame timing. Refer to Programmable Timer Clock Register section described above. Note: The user can only change the clock frequency source before starting the EXC-1553VME/MCH (i.e., setting STEX bit to '1').
9	ERTO	Extended Response Time-Out. Assertion of this bit enables the extended response time-out option and forces the BC Mode to look for an RTs response time in 30 usec or generate time-out errors. Negation of this bit enables for the standard time-out in 14 usec.
8-5	reserved	Should be set to '0'.
4	BCEN	Broadcast Enable. Assertion of this bit enables the broadcast option for BC Mode. Negation of this bit enables the remote terminal address 31 as a unique RT address. When enabled, the EXC-1553VME/MCH does not expect a status word response from the remote terminal.
3	reserved	Should be set to '0'.

Bit	Name	Description
2	PPEN	Ping-Pong Enable. This bit controls the method by which the EXC-1553VME/MCH will retry messages. A logic one allows the EXC-1553VME/MCH to ping-pong between buses during retries. A logic zero dictates that all retries will be performed on the programmed bus as defined in the Retry Number field of the Command Block control word.
1	INTEN	Interrupt Log List Enable. Assertion of this bit enables the Interrupt Log List. Negation of this bit prevents the logging of interrupts as they occur.
0	reserved	Should be set to '0'.

6.1.1.2 Operational Status Register 0002 (H) Read/Write

This register provides pertinent status information for BC Mode and is not reset to 0000H on reset. Instead the bit A/B_STD is set to '1'.

Note: To make changes to the BC and to this register, the STEX bit (Control Register, bit 15) must be logic zero.

Bit	Name	Description
15-10	reserved	Should be set to '0'.
9	MSEL1	Mode Select 1. In conjunction with Mode Select 0, this bit determines the channel's mode of operation.
8	MSEL0	Mode Select 0. In conjunction with Mode Select 1, this bit determines the channel's mode of operation.

MSEL1	MSEL0	Mode of Operation
0	0	BC Mode
0	1	RT Mode
1	0	BM Mode
1	1	RT/ Concurrent BM Mode

7	A/B_STD	Military Standard 1553A or 1553B. This bit determines whether the EXC-1553VME/MCH will operate under MIL-STD-1553A or 1553B protocol. Assertion of this bit forces the EXC-1553VME/MCH to look for all responses in 9 usec or generate time-out errors. Negation of this bit automatically allows the EXC-1553VME/MCH to operate under the MIL-STD-1553B protocol. See 'MIL-STD-1553A Operation' for further information.
6-4	reserved	These read-only bits are not applicable.
3	EX	EXC-1553VME/MCH Channel Executing. This read-only bit indicates whether the channel is presently executing or is idle. A logic one indicates that the channel is executing; logic zero indicates the channel is idle.
2	reserved	This read-only bit is not applicable.

Bit	Name	Description
1	READY	Channel Ready. This read-only bit indicates that the channel has completed initialization or B.I.T. This bit is cleared on reset.
0	TERACT	Channel Terminal Active. This read-only bit indicates that the channel is presently processing a 1553 message. This bit is cleared on reset.

Note: When STEX transitions from 1 to 0, EX and TERACT stay active until command processing is complete.

6.1.1.3 Current Command Register 0004 (H) - READ ONLY

This register contains the last 1553 command that was transmitted by the EXC-1553VME/MCH. Upon the execution of each Command Block, this register will automatically be updated. This register is updated when transmission of the Command Word begins. In an RT-RT transfer, the register will reflect the latest Command Word as it is transmitted.

Bit	Name	Description
15-0	CC[15-0]	Current Command. These bits contain the latest 1553 command that was transmitted by the bus controller.

6.1.1.4 Interrupt Mask Register 0006 (H) Read/Write

The BC Mode interrupt architecture allows the host to mask or temporarily disable the service of interrupts. While masked, interrupt activity does not occur. The unmasking of an interrupt after the event occurs, does not generate an interrupt for that event. An interrupt is masked only if the corresponding bit of this register is set to a logic zero.

Bit	Name	Description
15-12	reserved	Should be set to '0'.
11	MERR	Message Error Interrupt.
10-6	reserved	Should be set to '0'.
5	EOL	End Of List Interrupt.
4	ILLCMD	Illogical Command Interrupt.
3	ILLOP	Illogical Opcode Interrupt.
2	RTF	Retry Fail Interrupt.
1	CBA	Command Block Accessed Interrupt.
0	reserved	Should be set to '0'.

6.1.1.5 Pending Interrupt Register 0008 (H) - READ-ONLY

This register is used to identify which of the interrupts occurred during operation. The assertion of any bit in this register generates an interrupt. Note that all register bits are cleared on a host read.

Bit	Name	Description
15-12	reserved	Ignore on read.
11	MERR	Message Error Interrupt. Assertion of this bit indicates the occurrence of a message error. The EXC-1553VME/MCH can detect Manchester, sync-field, word count, 1553 word parity, bit count, and protocol errors. This bit will be set and an interrupt generated (if not masked) after message processing is complete.
10-6	reserved	Ignore on read.
5	EOL	End Of List Interrupt. Assertion of this bit indicates that the EXC-1553VME/MCH is at the end of the command block.
4	ILLCMD	Illogical Command Interrupt. Assertion of this bit indicates that an illogical command (i.e., Transmit Broadcast or improperly formatted RT-RT message) has been written into the Command Block. The EXC-1553VME/MCH checks for RT-RT Terminal address field match, RT-RT transmit/receive bit mismatch and correct order, and broadcast transmit commands. If illogical commands occur, the EXC-1553VME/MCH will halt execution.
3	ILLOP	Illogical Opcode Interrupt. Assertion of this bit indicates an illogical opcode (i.e., any reserved opcode) was used in the command block. The EXC-1553VME/MCH halts operation if this condition occurs.
2	RTF	Retry Fail Interrupt. Assertion of this bit indicates all programmed retries failed.
1	CBA	Command Block Accessed Interrupt. Assertion of this bit indicates a command block was accessed (Opcode 1010), if enabled.
0	reserved	Ignore on read.

6.1.1.6 Interrupt Log List Pointer Register 000A (H) Read/Write

The Interrupt Log List Pointer indicates the starting address of the Interrupt Log List. The Interrupt Log List is a 32-word ring-buffer that contains information pertinent to the service of interrupts. The EXC-1553VME/MCH architecture requires the location of the Interrupt Log List on a 32-word boundary. The most significant 11 bits of this register designate the location of the Interrupt Log List within a 64K memory space. Initialize the lower five-bits of this register to a logic zero. The EXC-1553VME/MCH controls the lower five-bits to implement the ring-buffer architecture. This register is read to determine the location and number of interrupts within the Interrupt Log List (least significant five-bits).

Bit	Name	Description
15-0	ILLP[15-0]	Interrupt Log List Pointer Bits.
		Note: Bits 15-5 indicate the starting Base address while bits 4-0 indicate the ring location of the Interrupt Log List.

6.1.1.7 BIT Word Register 000C (H) Read/Write

This register contains information on the current health of the channel hardware. The lower 8 bits of this register are user-defined.

Bit	Name	Description
15	DMAF	DMA Fail. Assertion of this bit indicates that all channel's internal DMA activity had not been completed within 16 usec.
14	WRAPF	Wrap Fail. The EXC-1553VME/MCH automatically compares the transmitted word (encoder word) to the reflected decoder word by way of the continuous loop-back feature. If the encoder word and reflected word do not match, the WRAPF bit asserts. The loop-back path is via the MIL-STD-1553 bus transceiver.
13	reserved	Ignore on read.
12	BITF	BIT Fail. Assertion of this bit indicates a B.I.T. failure. Interrogate bit 11 and 10 to determine the specific bus that failed.
11	BUAF	Bus A Fail. Assertion of this bit indicates a B.I.T. failure in Bus A.
10	BUBF	Bus B Fail. Assertion of this bit indicates a B.I.T. failure in Bus B.

Bit	Name	Description
9	MSBF	Memory Test Fail. Most significant memory byte failure.
8	LSBF	Memory Test Fail. Least significant memory byte failure.
7-0	UDB[7-0]	User-Defined Bits.

6.1.1.8 Minor Frame Timer Register 000E (H) - READ-ONLY

The Minor Frame Timer Register (MFT) reflects the state of the 16-bit MFT counter. This counter is loaded via the Load Minor Frame Timer opcode (Opcode 1110). For user-defined counter resolution use PTCE bit (Control Register, bit 10).

Bit	Name	Description
15-0	MFT[15-0]	Minor Frame Timer. These bits indicate the value of the timer.

6.1.1.9 Command Block Pointer Register 0010 (H) Read/Write

This register contains the location to start the Command Blocks. After execution begins, this register is automatically updated with the address of the next block.

Bit	Name	Description
15-0	CBA[15-0]	Command Block Address. These bits indicate the starting location of the Command Block.

6.1.2 BC Architecture

As defined in MIL-STD-1553, the bus controller initiates all communications on the bus. To meet MIL-STD-1553 bus controller requirements, the EXC-1553VME/MCH utilizes a Command Block architecture that takes advantage of both control registers and RAM.

Each command word transmitted over the bus must be associated with a Command Block. The Command Block requires eight contiguous 16-bit memory locations for each message. These eight locations include a control word, two command word locations, a data pointer (which indicates where data is to be written to or read from), two status word locations, a branch address location, and a timer value (used in the scheduling of messages). The host must initialize each of the locations associated with each Command Block (the exception being is for the two status locations which will be updated as command words are transmitted and corresponding status words are received). Command Blocks may be linked together in such a manner as to allow the generation of Major and Minor message frames. In addition, the BC can detect the assertion of Status Word bits and generate interrupts or branch to a new message frame, depending of course, on the specific conditions which arise.

6.1.2.0 BC Mode Command Block

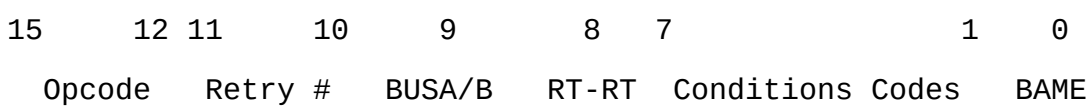
Figure 8 shows the BC's Command Block architecture while next sections describe each location associated with the Command Block.

Timer Value	eighth location
Branch Address	
Status Word 2	
Status Word 1	
Data Pointer	
Command Word 2	
Command Word 1	second location
Control Word	first location

Figure 8. BC Command Block Architecture

6.1.2.1 Control Word

The first memory location of each BC Mode Command Block contains the control word. Each control word contains the opcode, retry number, bus definition, RT-RT instruction, condition codes, and the block access message error. The control word is as follows:



Bit Number Description

15-12 Opcode. These bits define the opcode to be used by the EXC-1553VME/MCH for that particular Command Block. If the opcode does not perform any 1553 function, all other bits are ignored. Each of the available opcodes is defined in the next section.

11-10 Retry Number. These bits define the number of retries for each individual Command Block and if a retry opcode is used. If the Ping-Pong Enable Bit (bit 2 of the Control Register) is not enabled, all retries will occur on the programmed bus. However, if bit 2 is enabled, the first retry will always occur on the alternate bus, the second retry will occur on the primary bus, the third retry will occur on the alternate bus, and the fourth retry will occur on the primary bus.

BIT 11	BIT 10	# of Retries
0	1	1
1	0	2
1	1	3
0	0	4

9 Bus A/B. This bit defines on which of the two buses the command will be transmitted (i.e., primary bus). (Logic 1 = Bus A, Logic 0 = Bus B).

8 RT-RT Transfer. This bit defines whether or not the present Command Block is an RT-RT transfer and if the EXC-1553VME/MCH should transmit the second command word. Data associated with an RT-RT is always stored by the EXC-1553VME/MCH.

7-1 Condition Codes. These bits define the condition code the EXC-1553VME/MCH uses for that particular Command Block. Each of the available condition codes are defined in the following sections.

0 Block Access Message Error. Assertion of this bit indicates a protocol message error occurred in the RT's response. For this occurrence, the EXC-1553VME/MCH will overwrite this bit prior to storing the Control Word into memory. Noise on the 1553 bus may be one example of such an error.

6.1.2.1.1 BC Opcode Definition

Opcode (15-12)	Definition
0000	End Of List. This opcode instructs the EXC-1553VME/MCH that the end of the command block has been encountered. Command processing stops and the interrupt is generated if the interrupt is enabled. No command processing takes place (i.e., no 1553).
0001	Skip. This opcode instructs the EXC-1553VME/MCH to load the message-to-message timer with the value stored in the timer value location. The EXC-1553VME/MCH will then wait the specific time before proceeding to the next command block. This opcode allows for scheduling a specific time between message execution. No command processing takes place (i.e, no 1553).
0010	Go To. This opcode instructs the EXC-1553VME/MCH to "go to" the command block as specified in the branch address location. No command process takes place (i.e., no 1553).
0011	Built-in Test. This opcode instructs the channel to perform an internal built-in test. If the channel passes the built-in test, then processing of the next command block will continue. However if the channel fails the built-in test, then processing stops. No command processing takes place (i.e., no 1553).
0100	Execute Block; Continue. This opcode instructs the EXC-1553VME/MCH to execute the current command block and proceed to the next command block. This opcode allows for continuous operations.
0101	Execute Block; Branch. This opcode instructs the EXC-1553VME/MCH to execute the current command block and unconditionally branch to the location as specified in the branch address location.
0110	Execute Block; Branch on Condition. This opcode instructs the EXC-1553VME/MCH to execute the current command block and branch only if the condition is met. If no conditions are met, the opcode appears as an execute and continue.
0111	Retry on Condition. This opcode instructs the EXC-1553VME/MCH to perform automatic retries, as specified in the control word, if particular conditions occur. If no conditions are met, the opcode appears as an execute and continue.
1000	Retry on Condition; Branch. This opcode instructs the EXC-1553VME/MCH to perform automatic retries, as specified in the control word, if particular conditions occur. If the conditions are met, the EXC-1553VME/MCH retries. Once all retries have executed, the EXC-1553VME/MCH branches to the location specified in the branch address location. If no conditions are met, the opcode appears as an execute and branch.

Opcode	Definition
1001	Retry on Condition; Branch if all Retries Fail. This opcode instructs the EXC-1553VME/MCH to perform automatic retries, as specified in the control word, if particular conditions occur. If the conditions are met and all the retries fail, the EXC-1553VME/MCH branches to the location as specified in the branch address location. If no conditions are met, the opcode appears as an execute and continue.
1010	Interrupt; Continue. This opcode instructs the EXC-1553VME/MCH to interrupt and continue processing on the next command block. When using this opcode, no 1553 processing occurs.
1011	Call. This opcode instructs the EXC-1553VME/MCH to "go to" the command block as specified in the branch address location without processing this block. The next command block address is saved in an internal register so that the EXC-1553VME/MCH may remember one address and return to the next command block. No command processing takes place (i.e., no 1553).
1100	Return to Call. This opcode instructs the EXC-1553VME/MCH to return to the command block address saved during the Call opcode. No command processing takes place (i.e., no 1553).
1101	Reserved. The EXC-1553VME/MCH will generate an illegal opcode interrupt (if interrupt enabled) and automatically stop execution if a reserved opcode is used.
1110	Load Minor Frame Timer. This opcode instructs the EXC-1553VME/MCH to load the minor frame timer (MFT) with the value stored in the eighth location of the current command block. The timer will be loaded after the previous MFT has decremented to zero. After the MFT timer is loaded with the new value, the EXC-1553VME/MCH will proceed to the next command block. No command processing takes place (i.e., no 1553).
1111	Return to Branch. This opcode instructs the EXC-1553VME/MCH to return to the command block address saved during a Branch opcode. No command processing takes place (i.e., no 1553).

Note: For retries with interrupts enabled, all interrupts are logged after message processing is complete.

6.1.2.1.2 BC Condition Codes

Condition codes have been provided as a means for the EXC-1553VME/MCH to perform certain functions based on the RT's status word. In an RT-RT transfer, the conditions apply to both of the status words. Each bit of the condition codes is defined below.

Bit Number	Description
7	Message Error. This condition will be met if the EXC-1553VME/MCH detects an error in the RT's response, or if it detects no response. (The EXC-1553VME/MCH will wait 15 usec in 1553B mode and 11 usec in 1553A mode before declaring an RT no response).
6	Status Word Response with the Message Error bit set (Bit-time 9 in 1553A mode). This condition is met if the EXC-1553VME/MCH detects that the RT's status word has the Message Error bit set.
5	Status Word Response with the Busy bit set (Bit-time 16 in 1553A mode). This condition is met if the EXC-1553VME/MCH detects that the RT's status word has the Busy bit set.
4	Status Word Response with the Terminal Flag bit set (Bit- time 19 in 1553A mode). This condition is met if the EXC-1553VME/MCH detects that the RT's status word has the Terminal Flag bit set.
3	Status Word Response with the Subsystem Fail bit set (Bit-time 17 in 1553A mode). This condition is met if the EXC-1553VME/MCH detects that the RT's status word has the Subsystem Fail bit set.
2	Status Word Response with the Instrumentation bit set (Bit-time 10 in 1553A mode). This condition is met if the EXC-1553VME/MCH detects that the RT's status word has the Instrumentation bit set.
1	Status Word Response with the Service Request bit set (Bit-time 11 in 1553A mode). This condition is met if the EXC-1553VME/MCH detects that the RT's status word has the Service Request bit set.

6.1.2.2 1553 Command Words

The next two locations of the BC Mode Command Block are for 1553 command words. In most 1553 messages, only the first command word needs to be initialized. However, in an RT-RT transfer, the first command word is the Receive Command and the second command word is the Transmit Command.

6.1.2.3 Data Pointer

The fourth location of the BC Mode Command Block is the data pointer that points to the first memory location to store or fetch the data words associated with the message for that command block. This data structure allows the EXC-1553VME/MCH to store or fetch the exact specified number of data words, thus saving memory space and providing efficient space allocation. (Note: In an RT-RT transfer, the EXC-1553VME/MCH uses the data pointer as the location in memory to store the transmitted data in the transfer.) One common application for the data pointer occurs when the EXC-1553VME/MCH needs to send the same data words to several RTs. Here, each Command Block associated with those messages would contain the same data pointer value, and, therefore, fetch and transmit the same data. Note that the Data Pointer is never updated (i.e., the EXC-1553VME/MCH reads and writes the pointer but never changes its value).

6.1.2.4 1553 Status Words

The next two locations in the BC Mode Command Block are for status words. As the RT responds to the BC's command, the corresponding status word will be stored in Status Word 1. In an RT-RT transfer, the first status word will be the status of the Transmitting RT while the second status word will be the status of the Receiving RT.

6.1.2.5 Branch Address

The seventh location in the BC Mode Command Block contains the starting location of the branch. This location simply allows the EXC-1553VME/MCH to branch to another location in memory when certain opcodes are used.

6.1.2.6 Timer Value

The last location in the BC Mode Command Block is the Timer Value. This timer is used for one of two purposes.

First, the value may be used to set up minor frame schedules when using the Load Minor Frame Timer opcode (1110). The MFT counter may be driven by the Programmable Timer Clock. If not driven by the Programmable Timer Clock, the MFT counter is clocked by a fixed 15.625 KHz (64 usec) clock. The MFT counter runs continuously during message processing and must decrement to zero prior to loading the next Minor Frame time value.

Second, the value may be used as a message-to-message timer (MMT) when using the Skip opcode (0001). The MMT timer is clocked at a 24.0 MHz (41.666.. nsec) rate and allows for scheduling a specific time between message execution.

6.1.3 Command Block Chaining

The user determines the first Command Block by setting the initial start address in the Command Block Pointer Register. The Command Blocks will execute in a contiguous fashion as long as no "go to", "branch", "call", or "return" opcodes are used. With the use of these opcodes, almost any memory configuration is possible. Figures 9, 10, and 11 show how several Command Blocks may be linked together to form a command frame and how branch opcodes may be used to link minor frames. The minimum BC intermessage gap is 28.0 usec.

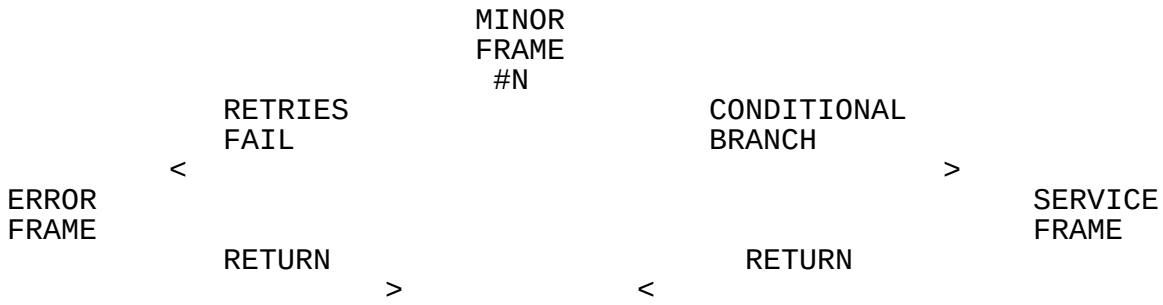


Figure 9. BC Minor Frame Branching

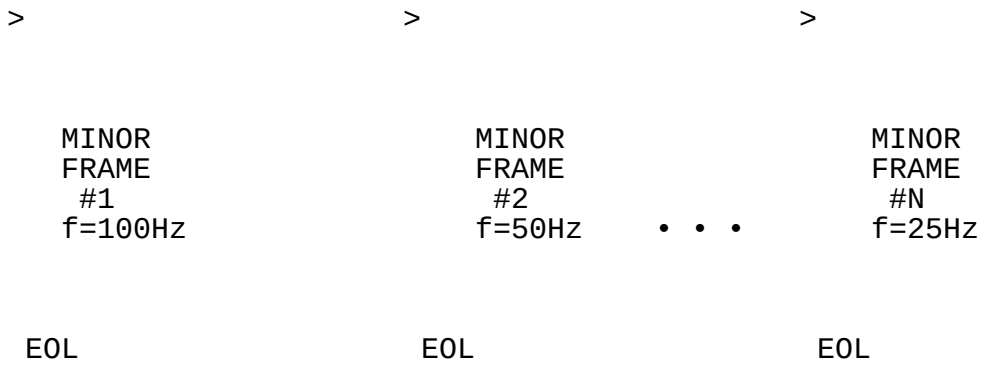


Figure 10. BC Minor Frame Sequencing

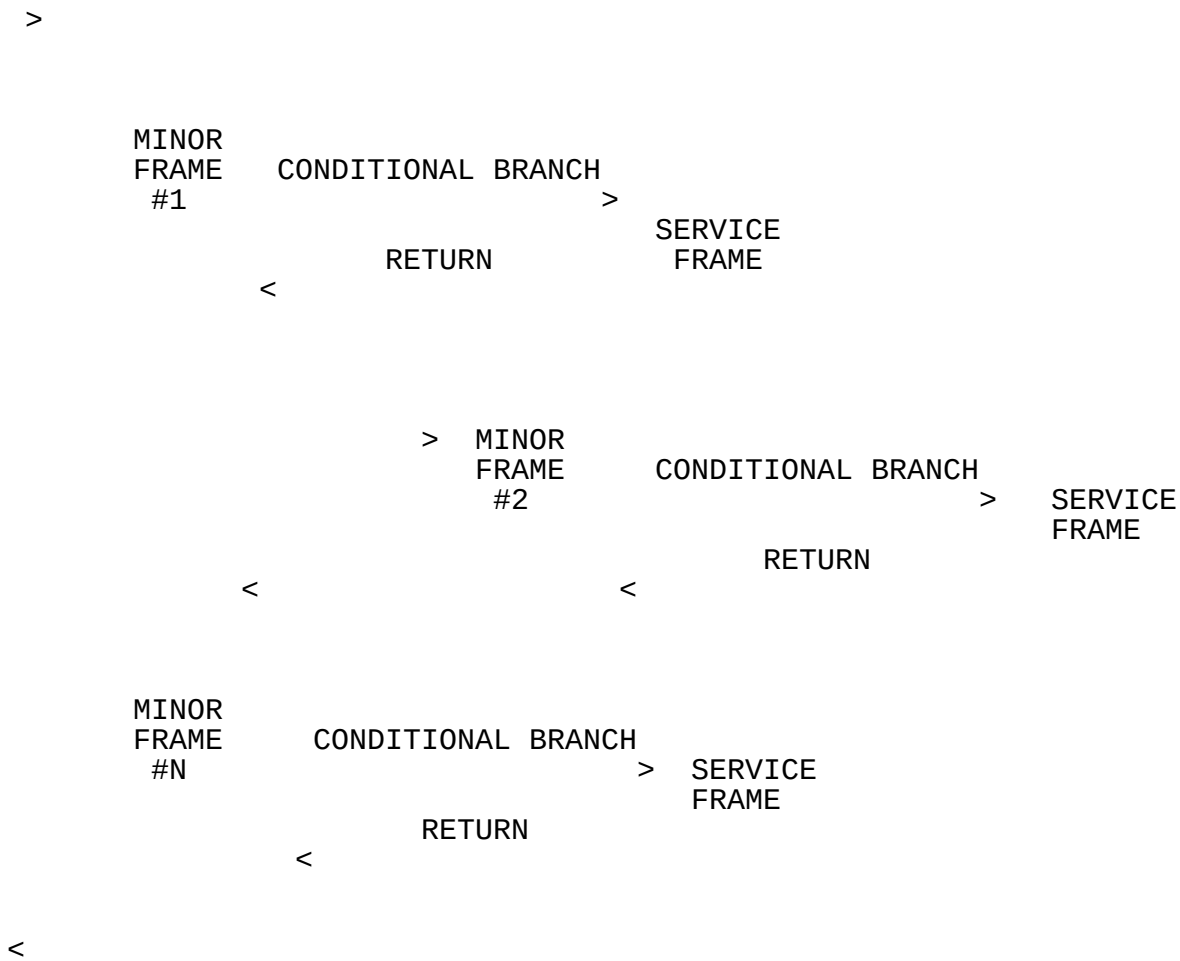


Figure 11. BC Major Frame Sequencing

6.1.4 Memory Architecture

After reviewing the control registers, it may be advantageous to look at how the user sets up memory to configure the EXC-1553VME/MCH in bus controller mode. The intent of this section is to show one method for defining the memory configuration.

The configuration shows the Command Blocks, data locations, and the Interrupt Log List as separate entities. Figure 12 shows that the first block of memory is allocated for the Command Blocks. Notice that the Command Block Pointer Register initially points to the control word of the first Command Block. After completing execution for that first Command Block, the Command Block Pointer Register will automatically be updated to show the address with the next Command Block.

Following the Command Block locations is the memory required for all the data words. In BC applications, the number of data words for each Command Block is known. In figure 12, for example, the first Command Block has allocated several memory locations for expected data. Conversely, the second Command Block has only allocated a few memory locations. Since the number of data words associated with each Command Block is known, memory may be used efficiently.

Also shown as a separate memory area is the Interrupt Log List (refer to the description of the Interrupt Log List). Notice that the Interrupt Log List Pointer Register points to the top of the initial Log List. After execution of that first BC Command Block, the Interrupt Log List Pointer Register will automatically be updated.

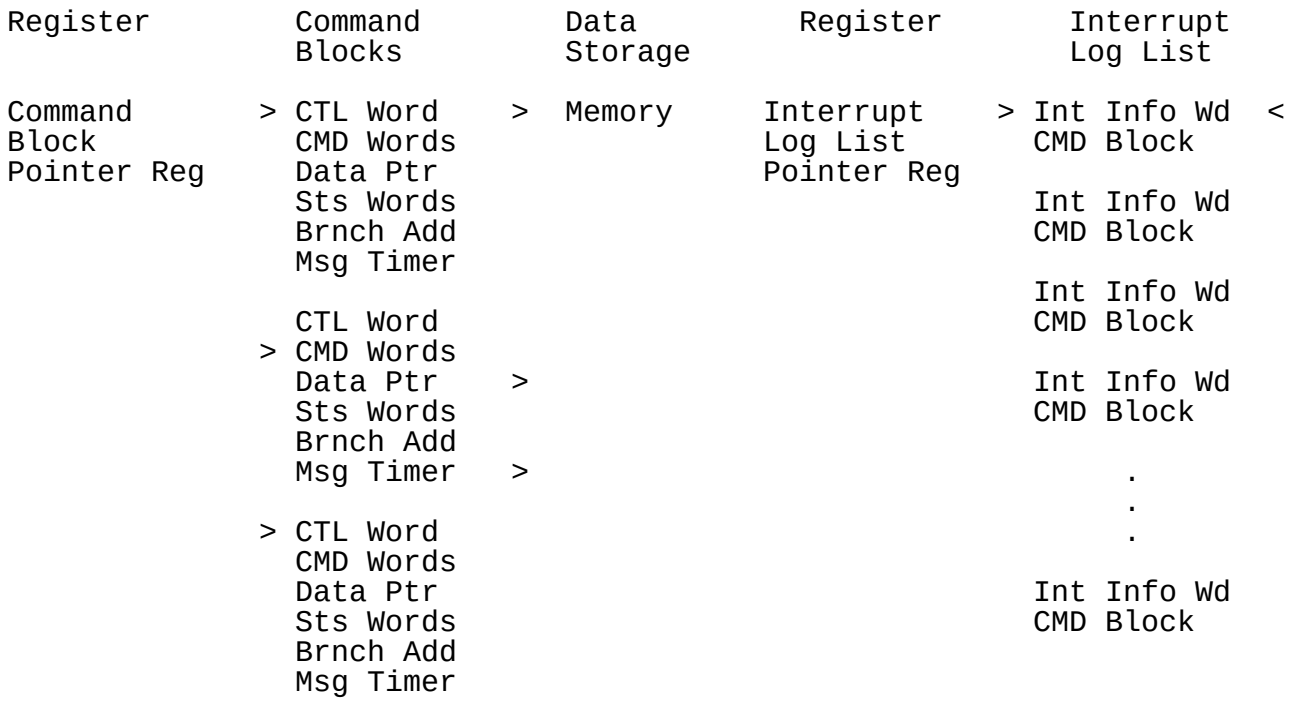


Figure 12. BC Memory Architecture

6.1.5 Message Processing

To process messages, the EXC-1553VME/MCH uses data supplied in the control registers along with data stored in memory. The EXC-1553VME/MCH accesses eight words stored in memory called a command block. The command block is accessed at the beginning and end of command processing.

Note: In BC mode, the EXC-1553VME/MCH does not need to re-read the Command Block on a retry situation.

The user allocates memory spaces for the minor frame. The top of the command blocks can reside at any address location. Defined and entered into memory by the user, the control registers are linked to the Command Block via the Command Block Pointer Register contents. Each command block contains a Control Word, Command Word 1, Command Word 2, Data Pointer, Status Word 1, Status Word 2, Branch Address, and Timer Value. Refer to the previous sections for a complete description of each location.

Control word information allows the EXC-1553VME/MCH to control the commands transmitted over the 1553 bus. The Control word allows the EXC-1553VME/MCH to transmit commands on a specific bus, perform retries, initiate RT-RT transfers, and interrupt on certain conditions. The host defines each command word associated with each command block. For normal 1553 commands, only the first command word location will contain valid data. For RT-RT commands, as specified in the Control word, the host must define the first command word as a receive and the second command word as a transmit.

For a receive command the Data Pointer is read to determine where data words are retrieved. The EXC-1553VME/MCH retrieves data words sequentially from the address specified by the Data Pointer. For a transmit command the Data Pointer is read to determine the top memory location. The EXC-1553VME/MCH stores data words sequentially from this top memory location.

The EXC-1553VME/MCH reads the command block during minor frame processing. The EXC-1553VME/MCH then begins the acquisition of data words for either transmission or storage.

After transmission or reception, the EXC-1553VME/MCH begins post-processing. The command block is updated. The EXC-1553VME/MCH modifies the Control word as required. An optional interrupt log entry is performed after the command block update.

6.1.6 MIL-STD-1553A Operation

The EXC-1553VME/MCH may be configured to meet the MIL-STD-1553A protocol. When configured as a MIL-STD-1553A bus controller, the EXC-1553VME/MCH will operate as follows:

- Looks for the RT response within 9 usec;
- Defines all mode codes without data;
- Defines subaddress 00000 as a mode code;

A/B_STD	ERTO	RESULT
0	0	1553B standard, 1553B response (in 14 usec)
0	1	1553B standard, extended response (in 30 usec)
1	0	1553A standard, 1553A response (in 9 usec)
1	1	1553A standard, extended response (in 21 usec)

6.2 REMOTE TERMINAL MODE (RT MODE)

6.2.1 Control Registers for RT Mode

The control registers are read/write unless otherwise stated. All control registers **must** be accessed in word mode. All control register bits are active high and are reset to '0' unless otherwise stated.

	003E (H)
ILLEGALIZATION REGISTERS [16 registers]	0020 (H)
	001E (H)
reserved	
	0014 (H)
1553 STATUS WORD BITS REG	0012 (H)
RT DESCRIPTOR POINTER REG	0010 (H)
TIME TAG REGISTER	000E (H)
BIT WORD REG	000C (H)
INT LOG LIST POINTER REG	000A (H)
PENDING INTERRUPT REG	0008 (H)
INTERRUPT MASK REG	0006 (H)
CURRENT COMMAND REG	0004 (H)
OPERATIONAL STATUS REG	0002 (H)
CONTROL REGISTER	0000 (H)

Figure 13. RT Control Registers Map

6.2.1.0 Description of RT Mode Control Registers

6.2.1.1 Control Register 0000 (H) Read/Write

The Control Register controls RT Mode configuration. To make changes to the RT Mode and this register, the STEX bit (Bit 15) must be logic zero.

Bit	Name	Description
15	STEX	Start Channel Execution. Assertion of this bit initiates operation of the EXC-1553VME/MCH channel. A Control Register write negating this bit inhibits channel operation. A remote terminal address parity error prevents RT Mode operation regardless of the logical state of this bit. If an RT address parity error exists, bit 3 of the Operational Status Register will be set low and bit 2 of the Operational Status Register will be set high.
14	SBIT	Start Channel B.I.T. Assertion of this bit places the channel into the Built-In Test routine. The BIT test takes 1 ms to execute and has a fault coverage of 93.4%. If the channel has been started, the host must halt the channel in order to place the channel into the Built-In Test routine (STEX = 0). Note: If Start B.I.T. (SBIT) and Start Execution (STEX) are both set on one register write, SBIT has priority.
13	reserved	Should be set to '0'.
12	BUAEN	Bus A Enable. Setting this bit enables Bus A operation. If negated, the EXC-1553VME/MCH does not recognize commands received over Bus A.
11	BUBEN	Bus B Enable. Setting this bit enables Bus B operation. If negated, the EXC-1553VME/MCH does not recognize commands received over Bus B.
10	PTCE	Programmable Timer Clock Enable. Assertion of this bit enables a programmable clock used with an internal time-tag counter. Refer to Programmable Timer Clock Register section described above. Note: The user can only change the clock frequency source before starting the EXC-1553VME/MCH (i.e., setting STEX bit to '1').
9	PPACK	Ping-Pong Acknowledge. This read-only bit acknowledges the Ping-Pong operation. The Ping-Pong Enable is acknowledged by transitioning from a logical zero to a logical one, while the Ping-Pong Disable is acknowledged by transitioning from a logical one to a logical zero.

Bit	Name	Description
8-7	RTM[1-0]	Remote Terminal Mode bits. These two bits determine the RT mode of operation.

RTM[1-0]	RT Mode
0 0	Mode #0 (Index or Ping-Pong Operation)
0 1	X (reserved)
1 0	Mode #1 (Circular Buffer 1 Operation)
1 1	Mode #2 (Circular Buffer 2 Operation)

5	reserved	Should be set to '0'.
4	BCEN	Broadcast Enable. Assertion of this bit enables the broadcast option for RT Mode. Negation of this bit enables remote terminal address 31 as a unique remote
3	DYNBC	Dynamic Bus Control Acceptance. This bit controls the EXC-1553VME/MCH's ability to accept the dynamic bus control mode code. Assertion of this bit allows the EXC-1553VME/MCH to respond to a dynamic bus control mode code with status word bit 18 set to a logic one. Negation of this bit prevents the assertion of status word bit 18 upon reception of the dynamic mode code.
2	PPEN	Ping-Pong Enable. Assertion of this bit enables the ping-pong buffer feature of the EXC-1553VME/MCH and disables the message indexing feature. Negation of this bit disables the ping-pong feature and enables the message indexing feature.
1	INTEN	Interrupt Log Enable. Assertion of this bit enables the interrupt logging feature. Negation of this bit prevents the logging of interrupts.
0	XMTSW	Transmit Last Status Word. Assertion of this bit allows the EXC-1553VME/MCH to automatically execute the TRANSMIT LAST STATUS WORD mode code when configured for MIL-STD-1553A mode operation.

6.2.1.2 Operational Status Register 0002 (H) Read/Write

This register provides pertinent status information for RT Mode and is not reset to 0000H on reset. Instead the bits A/B_STD, and RTA[4-0] are set to '1'.

Note: To make changes to the RT and to this register, the STEX bit (Control Register, bit 15) must be logic zero.

Bit	Name	Description
15-11	RTA[4-0]	Remote Terminal Address Bits. These five bits contain the remote terminal address. The RTA4 bit is the MSB bit, while the RTA0 bit is the LSB bit.

Bit	Name	Description
10	RTAPTY	Terminal Address Parity Bit. This bit is appended to the remote terminal address bus (RTA[4-0]) to supply odd parity. The EXC-1553VME/MCH requires odd parity for proper operation.
9	MSEL1 Mode	Select 1. In conjunction with Mode Select 0, this bit determines the channel's mode of operation.
8	MSEL0 Mode	Select 0. In conjunction with Mode Select 1, this bit determines the channel's mode of operation.

MSEL1	MSEL0	Mode of Operation
0	0	BC Mode
0	1	RT Mode
1	0	BM Mode
1	1	RT/ Concurrent BM Mode

7	A/B_STD	Military Standard 1553A or 1553B. This bit determines whether the EXC-1553VME/MCH will operate under MIL-STD-1553A or 1553B protocol. Assertion of this bit enables the XMTSW bit (Bit 0 of the Control Register). Negation of this bit automatically allows the EXC-1553VME/MCH to operate under the MIL-STD-1553B protocol.
6-4	reserved	These read-only bits are not applicable.
3	EX	EXC-1553VME/MCH Channel Executing. This read-only bit indicates whether the channel is presently executing or is idle. A logic one indicates that the channel is executing; logic zero indicates the channel is idle.
2	TPARF	Terminal Parity Fail. This bit indicates the observance of a terminal address parity error. The EXC-1553VME/MCH checks for odd parity. This read only bit reflects the parity of Operational Status Register bits 15-10.
1	READY	Channel Ready. This read-only bit indicates that the channel has completed initialization or B.I.T. This bit is cleared on reset.
0	TERACT	Channel Terminal Active. This read-only bit indicates that the channel is presently processing a 1553 message. This bit is cleared on reset.

Note: Remote Terminal Address and Parity are checked on start of execution.

RT Mode

6.2.1.3 Current Command Register 0004 (H) - READ ONLY

This register contains the last valid 1553 command processed by the EXC-1553VME/MCH.

Bit	Name	Description
15-0	CC[15-0]	Current Command. These bits contain the latest valid 1553 command that was received by the EXC-1553VME/MCH. This register is valid 13 usec after TERACT is negated.

6.2.1.4 Interrupt Mask Register 0006 (H) Read/Write

The EXC-1553VME/MCH interrupt architecture allows for the masking of all interrupts. An interrupt is masked if the corresponding bit of this register is set to logic zero. This feature allows the host to temporarily disable the service of interrupts. While masked, interrupt activity does not occur. The unmasking of an interrupt after the event occurs does not generate an interrupt for that event.

Bit	Name	Description
15-12	resereved	Should be set to '0'
11	MERR	Message Error Interrupt
10	SUBAD	Subaddress Accessed Interrupt
9	BDRCV	Broadcast Command Received Interrupt
8	IXEQ0	Index Equal Zero Interrupt
7	ILLCMD	Illegal Command Interrupt
6-0	reserved	Should be set to '0'.

6.2.1.5 Pending Interrupt Register 0008 (H) - READ-ONLY

The Pending Interrupt Register contains information that identifies events which generate interrupts. The assertion of any bit in this register generates an interrupt. A register read of the Pending Interrupt Register will clear all bits.

Bit	Name	Description
15-12	reserved	Ignore on read.

Bit	Name	Description
11	MERR	Message Error Interrupt. Assertion of this bit indicates that a message error condition exists. The EXC-1553VME/MCH can detect manchester errors, sync-field, word count errors (too many or too few), MIL-STD-1553 word parity errors, bit count errors (too many or too few), and protocol errors. If not masked, this bit is always set and an interrupt generated when the EXC-1553VME/MCH asserts bit-time 9 (Message Error) of the 1553 status word (e.g., illegal commands, invalid data word, etc.).
10	SUBAD	Subaddress Accessed Interrupt. Assertion of this bit indicates a pre-selected subaddress has transacted a message. To determine the exact subaddress, the host interrogates the interrupt log IAW.
9	BDRCV	Broadcast Command Received Interrupt. This bit is set to a logic one to indicate the EXC-1553VME/MCH's receipt of a valid broadcast command. The EXC-1553VME/MCH suppresses status word transmission.
8	IXEQ0	Index Equal Zero Interrupt. The EXC-1553VME/MCH asserts this bit to indicate the completion of a pre-defined number of commands by the RT. Upon assertion of this interrupt, the host updates the subaddress descriptor to prevent the potential loss of data.
7	ILCMD	Illegal Command Interrupt. This bit is set to a logic one to indicate the reception of an illegal command by the EXC-1553VME/MCH. Upon receipt of this command, the EXC-1553VME/MCH responds with a status word only; Bit-time 9 (Message Error) of the 1553 status word is set to a logic one.
6-0	reserved	Ignore on read.

6.2.1.6 Interrupt Log List Pointer Register 000A (H) Read/Write

The Interrupt Log List Pointer indicates the starting address of the Interrupt Log List. The Interrupt Log List is a 32 word ring-buffer that contains information pertinent to the service of interrupts. The EXC-1553VME/MCH architecture requires the location of the Interrupt Log List on a 32-word boundary. The most significant 11 bits of this register designate the location of the Interrupt Log List within a 64K memory space. The lower 5 bits of this register should be initialized to a logic zero. The EXC-1553VME/MCH controls the lower 5 bits to implement the ring-buffer architecture. This register is read to determine the location and number of interrupts within the Interrupt Log List (least significant 5 bits).

Bit	Name	Description
15-0	ILLP[15-0]	Interrupt Log List Pointer Bits. Note: Bits 15-5 indicate the starting Base address while bits 4-0 indicate the ring location of the Interrupt Log List.

6.2.1.7 BIT Word Register 000C (H) Read/Write

This register contains information on the channel's hardware current health. The RT transmits the contents of this register upon reception of a Transmit BIT Word Mode Code. The lower 8 bits of this register are user-defined.

Bit	Name	Description
15	DMAF	DMA Fail. Assertion of this bit indicates that all channel's internal DMA activity had not been completed within 7 usec.
14	WRAPF	Wrap Fail. The EXC-1553VME/MCH automatically compares the transmitted word (encoder word) to the reflected decoder word via the continuous loop-back feature. If the encoder word and reflected word do not match, the WRAPF bit is asserts. The loop-back path is via the MIL-STD-1553 bus transceiver.
13	TAPF	Terminal Address Parity Fail. This bit reflects the outcome of the remote terminal address parity check. A logic one indicates a parity failure. When a parity error occurs the EXC-1553VME/MCH does not begin operation (STEX bit forced to a logic zero) and bus A and B do not enable.
12	BITF	BIT Fail. Assertion of this bit indicates a B.I.T. failure. Bits 11 and 10 should be interrogated to determine the specific bus that failed. 1553 status word bit-time 19 (Terminal Flag) is automatically set to a logic one when a B.I.T. failure occurs.
11	BUAF	Bus A Fail. Assertion of this bit indicates a B.I.T. failure in Bus A.
10	BUBF	Bus B Fail. Assertion of this bit indicates a B.I.T. failure in Bus B.
9	MSBF	Memory Test Fail. Most significant memory byte failure.
8	LSBF	Memory Test Fail. Least significant memory byte failure.
7-0	UDB[7-0]	User-Defined Bits.

6.2.1.8 Time-Tag Register 000E (H) - READ ONLY

The Time-Tag Register reflects the state of a 16-bit free running counter. This counter may be driven by the Programmable Timer Clock (see PTCE bit within Control Register). If not driven by the Programmable Timer Clock, this counter is clocked by a fixed 15.625 KHz (64 usec) clock. The Time-Tag counter is automatically reset when the EXC-1553VME/MCH receives a valid synchronize without data mode code. The EXC-1553VME/MCH automatically loads the Time-Tag counter with the data associated with reception of a valid synchronize with data mode code. The Time-Tag counter begins operation immediately after reset or within 64 usec; after the receipt of a valid mode code, reset remote terminal, or synchronize with/without data. When the RT is halted (STEX = 0), the Time-Tag continues to run.

Bit	Name	Description
15-0	TT[15-0]	Time-Tag Counter Bits. These bits indicate the state of the 16-bit internal counter.

6.2.1.9 RT Descriptor Pointer Register 0010 (H) Read/Write

Each subaddress and mode code has a reserved block of memory containing information on how to process a valid command to that subaddress or mode code. Located contiguously in memory, these reserved memory locations are called a descriptor space. The RT Descriptor Pointer Register contains an address that points to the top of this memory space. The EXC-1553VME/MCH uses the T/R bit, subaddress/mode code field, and mode code to select one block within the descriptor table for message processing. The RT Descriptor Pointer Register is static during message processing.

Bit	Name	Description
15-0	RTDA[15-0]	RT Descriptor Address Bits.

6.2.1.10 1553 Status Word Bits Register 0012 (H) Read/Write

This register controls the outgoing MIL-STD-1553 status word. The host controls the Instrumentation, Busy, Terminal Flag, Service Request, and Subsystem Flag by writing to bits 9 through 0 of this register. The EXC-1553VME/MCH's status word response reflects assertion of these bit(s) until negated by the host unless the Immediate Clear Function is enabled. The Immediate Clear Function automatically clears these bits after being transmitted in a status word.

The Immediate Clear Function does not affect the operation of the Transmit Last Status word and Transmit Last Command word Mode Codes. Transaction of a legal valid command with the INS bit set to a logic one and the Immediate Clear Function enabled, results in the transmission of a 1553 status word with Bit-time 10 asserted. If the ensuing command is a Transmit Last Status word or Last Command mode code, Bit-time 10 of the outgoing 1553 status word remains a logic one.

For MIL-STD-1553B applications, the register is as follows:

Bit	Name	Description
15	IMCLR	Immediate Clear Function. Assertion of this bit enables the Immediate Clear Function (IMF) of the EXC-1553VME/MCH. Enabling the IMF results in the clearing of the INS, BUSY, TF, SRQ, and/or SUBF bit immediately after a message is completed. This function is enabled by asserting this bit when asserting bit(s) INS, BUSY, TF, SRQ, and/or SSYSF. This bit should be used consistently since once set, it will remain set, and once cleared, it will remain cleared.
14-10	reserved	Should be set to '0'.
9	INS	Instrumentation Bit. This bit asserts the Instrumentation bit of the MIL-STD-1553B status word. (Bit-time 10 of the Status Word).
8	SRQ	Service Request Bit. This bit asserts the Service Request bit of the MIL-STD-1553B status word. (Bit-time 11 of the Status Word).
7-4	reserved	Should be set to '0'.
3	BUSY	Busy Bit. Assertion of this bit is reflected in the outgoing MIL-STD-1553B status word. Assertion of this bit prevents memory accesses. (Bit-time 16 of the Status Word).
2	SSYSF	Subsystem Flag Bit. This bit asserts the Subsystem Flag bit of the MIL-STD-1553B status word. (Bit-time 17 of the Status Word).
1	reserved	Should be set to '0'.
0	TF	Terminal Flag. Assertion of this bit is reflected in the outgoing MIL-STD-1553B status word. The EXC-1553VME/MCH automatically asserts this bit if a B.I.T. failure occurs. Inhibit Terminal Flag mode code prevents the assertion by the host. Override Inhibit Terminal Flag Mode Code re-establishes the Terminal Flag option (Bit-time 19 of the Status Word).

For MIL-STD-1553A applications, the register is as follows:

Bit	Name	Description
15	IMCLR	Immediate Clear Function. Assertion of this bit enables the Immediate Clear Function (IMF) of the EXC-1553VME/MCH. Enabling the IMF results in the clearing of the bit-times 10-19 immediately after a 1553 status word is transmitted. This function is enabled by asserting this bit when asserting bit-times 10-19. This bit should be used consistently since once set, it will remain set, and once cleared, it will remain cleared.
14-10	reserved	Should be set to '0'.
9	SB10	Status bit-time 10.
8	SB11	Status bit-time 11.
7	SB12	Status bit-time 12.
6	SB13	Status bit-time 13
5	SB14	Status bit-time 14.
4	SB15	Status bit-time 15.
3	SB16	Status bit-time 16.
2	SB17	Status bit-time 17.
1	SB18	Status bit-time 18.
0	SB19	Status bit-time 19.

6.2.1.11 Illegalization Registers 0020 (H) - 003E (H)

These 16 registers are divided into 8 blocks, 2 registers per block (see table 1).

Block Name	Address (H)
Receive	0020 and 0022
Transmit	0024 and 0026
Broadcast Receive	0028 and 002A
Broadcast Transmit (Automatically Illegalized)	002C and 002E
Mode Code Receive	0030 and 0032
Mode Code Transmit	0034 and 0036
Broadcast Mode Code Receive	0038 and 003A
Broadcast Mode Code Transmit	003C and 003E

Table 1. RT Illegalization Register Blocks

The blocks correspond to the following types of commands. Register address 0020 (H) and 0022 (H) illegalize receive commands to 32 subaddresses. The most significant bit of register 0020 (H) controls the illegalization of subaddress 01111. The least significant bit controls subaddress 00000. Register 0022 (H) controls illegalization of subaddresses 10000 through 11111. The least significant bit relates to subaddress 10000; the most significant bit relates to subaddress 11111. Transmit commands and broadcast commands (both receive and transmit) use the same encoding scheme as the receive subaddress illegalization.

Register 0030 (H) through 003E (H) control the illegalization of mode codes. Register 0030 (H) governs the illegalization of receive mode codes (T/R bit = 0) 00000 through 01111 and register 0032 (H) mode codes 10000 through 11111. Register blocks Transmit Mode Code (T/R bit = 1), Broadcast Receive Mode Codes, and Broadcast Transmit Mode Codes use the same decode scheme as the receive mode codes.

Table 2 shows the illegalization register map. For each block, the numbers shown in the column under each bit number identifies the specific subaddress or mode code (in hex) that the register bit illegalizes. (Logical 0 = legal, Logical 1 = illegal)

Name	Register Address(Hex)															
Bit Number		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Receive	0020	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
	0022	1F	1E	1D	1C	1B	1A	19	18	17	16	15	14	13	12	11	10
Transmit	0024	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
	0026	1F	1E	1D	1C	1B	1A	19	18	17	16	15	14	13	12	11	10
Brd Receive	0028	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
	002A	1F	1E	1D	1C	1B	1A	19	18	17	16	15	14	13	12	11	10
Brd Transmit	002C	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX
	002E	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX
Mode Receive	0030	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
	0032	1F	1E	1D	1C	1B	1A	19	18	17	16	15	14	13	12	11	10
Mode Transmit	0034	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
	0036	1F	1E	1D	1C	1B	1A	19	18	17	16	15	14	13	12	11	10
Mode Brd Receive	0038	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	UU	01	WW
	003A	1F	1E	1D	1C	1B	1A	19	18	17	16	15	14	13	12	11	10
Mode Brd Transmit	003C	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	ZZ	01	XX
	003E	YY	YY	YY	YY	YY	YY	YY	YY	YY	YY	YY	YY	YY	YY	YY	YY

Table 2. RT Illegalization Register Map

Notes:
1. Brd = Broadcast
2. Mode = Mode code

RT Mode

3. XX = Automatically illegalized by EXC-1553VME/MCH.
4. YY = Automatically illegalized by EXC-1553VME/MCH in 1553B only.
5. ZZ = Automatically illegalized by EXC-1553VME/MCH in 1553B and 1553A if XMTSW is enabled.
6. WW = Automatically illegalized in 1553A.
7. UU = Automatically illegalized in 1553A if XMTSW enabled.

6.2.2 Descriptor Block

To process messages, the EXC-1553VME/MCH uses data from the control registers with data stored in the RAM. The EXC-1553VME/MCH accesses a four word descriptor block stored in RAM. The descriptor block is accessed at the beginning and end of command processing. Multiple descriptor blocks are sequentially entered into memory to form a descriptor table. The following paragraphs discuss the descriptor block in detail.

The host controlling the EXC-1553VME/MCH allocates 512 consecutive memory spaces for the subaddress and mode code descriptor table (see figure 14). The top of the descriptor table can reside at any address location. The control registers are linked to the descriptor table via the Descriptor Address Register contents. Each descriptor block contains a Control Word, Data Pointer A, Data Pointer B, and Broadcast Data Pointer. Each subaddress and mode code is assigned a descriptor for receive and transmit commands (T/R bit equals zero or one).

Control word information allows the EXC-1553VME/MCH to generate interrupts, buffer messages, and control message processing. For a receive command, the Data List Pointer is read to determine the top of the data buffer. The EXC-1553VME/MCH stores data sequentially from the top of data buffer plus two locations (e.g., 0100H, 0102H, 0104H, 0106H, etc.). When processing a transmit command, the Data List Pointer is read to determine where data words are retrieved. The EXC-1553VME/MCH retrieves data words sequentially from the address the Data List Pointer designates plus two 16-bit address locations.

The Broadcast Data Pointer allows for separate storage of non-broadcast data from broadcast data per MIL-STD-1553B Notice II. The user enables or disables this feature via the Control Word's least significant bit. When disabled, the non-broadcast and broadcast data is stored via Data List Pointer A or B. For transmit commands, the Broadcast Data Pointer is not used. The EXC-1553VME/MCH does not transmit any information on the receipt of a broadcast transmit command.

The EXC-1553VME/MCH reads the descriptor block during command processing (i.e., after assertion of TERACT). The EXC-1553VME/MCH reads the control word and three Data Pointers. The EXC-1553VME/MCH then begins the acquisition of data words for either transmission or storage.

After transmission or reception, the EXC-1553VME/MCH begins post-processing. The Descriptor Block is updated. An optional interrupt log entry is performed after a descriptor update. During the descriptor update, the EXC-1553VME/MCH modifies the Control Word index field and bits 4, 2, and 1, if required. The EXC-1553VME/MCH updates Data Pointer A if no message errors occurred during the message transaction. Reception of a broadcast command, with no message errors, results in the update of the Broadcast Data Pointer. Neither Data Pointer A or B is updated if the EXC-1553VME/MCH has the ping-pong mode of operation enabled.

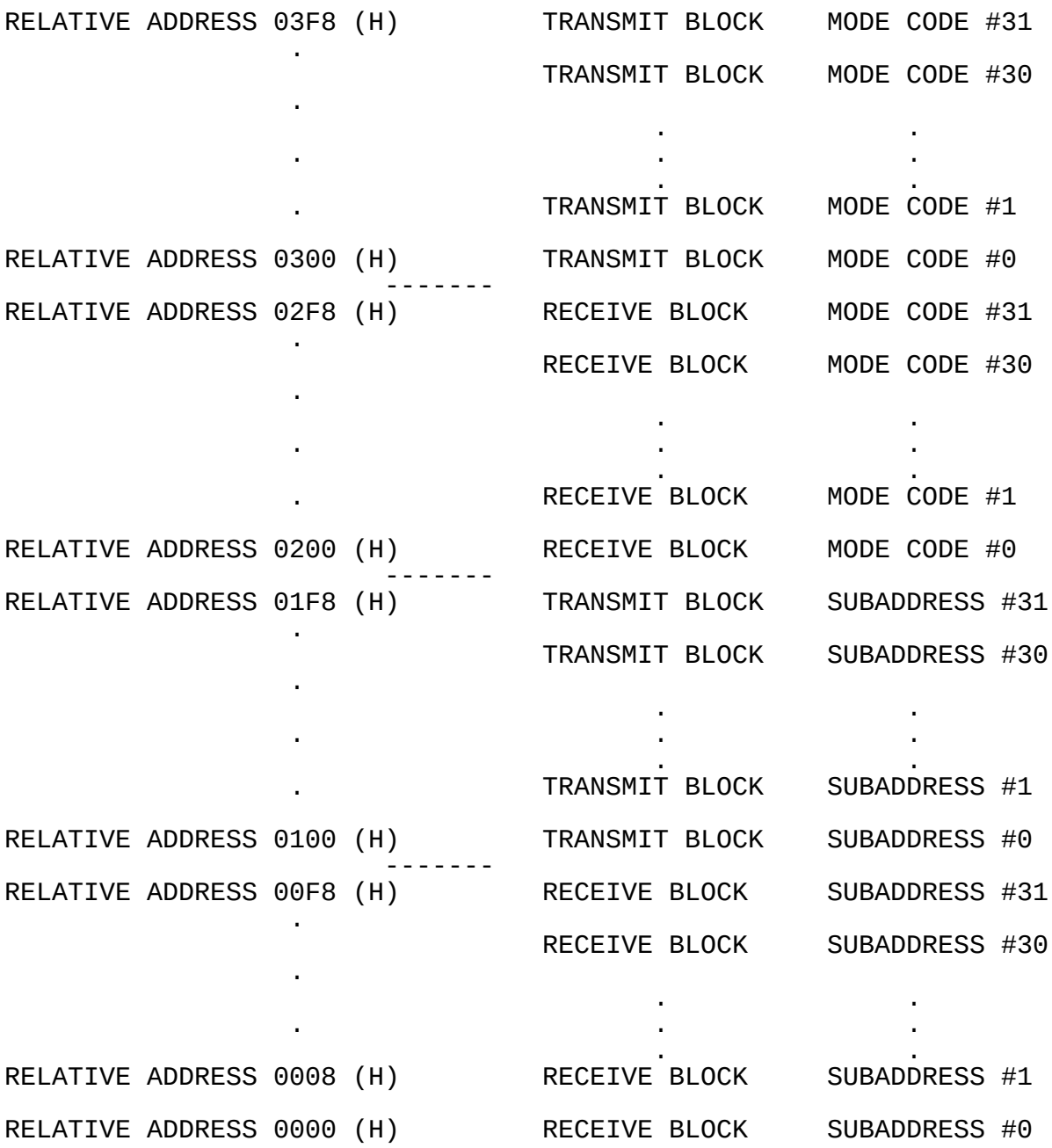


Figure 14. RT Descriptor Table

6.2.2.0 Descriptor Block Control Words

6.2.2.1 Receive Control Word

The following bits describe the receive subaddress descriptor Control word. Information contained in this word assists the EXC-1553VME/MCH in message processing. The descriptor control word is initialized by the host and updated by the EXC-1553VME/MCH during command post-processing.

Bit	Name	Description
15-8	INDX	Index Field. These bits define multiple message buffer length. The host uses this field to instruct the EXC-1553VME/MCH to buffer "N" messages. "N" can range from 0(00 H) to 256(FF H). If buffer ping-ponging is enabled, the INDX field is "don't care" (i.e., does not contain applicable information). During ping-pong mode operation, initialize the index field to 00 (H). The RT does not perform multiple message buffering in the ping-pong mode of operation. The index decrements each time a complete message is transacted (no message errors). The index does not decrement if the subaddress is illegalized. The EXC-1553VME/MCH can generate an interrupt when the index field transitions from one to zero (see bit 7).
7	INTX	Interrupt Index Equals Zero. Assertion of this bit enables the generation of an interrupt when the index field transitions from one to zero. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. An interrupt is generated after message processing.
6	IWA	Interrupt When Accessed. Assertion of this bit enables the generation of an interrupt when the subaddress receives a valid command. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. An interrupt is generated after message processing.
5	IBRD	Interrupt Broadcast Received. Assertion of this bit enables the generation of an interrupt when the subaddress receives a valid broadcast command. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. An interrupt is generated after message processing.
4	BAC	Block Accessed. The host initializes this bit to zero; the EXC-1553VME/MCH overwrites the zero with a logic one upon completion of message processing. After interrogating this bit, the host resets this bit to zero to observe further accesses.
3	reserved	Should be set to '0'.

Bit	Name	Description
2	A/B	Buffer A/B. Indicates the last buffer accessed when buffer ping-pong is enabled. During initialization, the host designates the first buffer used by asserting or negating this bit. A logic one indicates buffer A; a logic zero indicates buffer B. This bit is a "don't care" if buffer ping-ponging is not enabled.
1	BRD	Broadcast Received. Assertion of this bit indicates the reception of a valid broadcast command.
0	NII	Notice II. Assertion of this bit enables the use of the Broadcast Data Pointer as a buffer for broadcast command information. When negated, broadcast information is stored in the same buffer as non-broadcast information.

6.2.2.2 Transmit Control Word

The following bits describe the transmit subaddress descriptor Control word. Information contained in this word assists the EXC-1553VME/MCH in message processing. The descriptor control word is initialized by the host and updated by the EXC-1553VME/MCH during command post-processing.

Bit	Name	Description
15-7	reserved	Should be set to '0'.
6	IWA	Interrupt When Accessed. Assertion of this bit enables the generation of an interrupt when the subaddress receives a valid command. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. An interrupt is generated after message processing.
5	reserved	Should be set to '0'.
4	BAC	Block Accessed. The host initializes this bit to zero and the EXC-1553VME/MCH overwrites the zero with a logic one upon completion of message processing. After interrogation, the user should reset this bit to zero to observe further accesses.
3	reserved	Should be set to '0'.
2	A/B	Buffer A/B. Indicates the data pointer to access when buffer ping-pong is enabled. During initialization, the host designates the first buffer used by asserting or negating this bit. A logic one indicates buffer A; a logic zero indicates buffer B. This bit is a "don't care" if buffer ping-ponging is not enabled.

Bit	Name	Description
1	BRD	Broadcast Received. Assertion of this bit indicates the reception of a broadcast command.
0	reserved	Should be set to '0'.

6.2.2.3 Mode Code Receive Control Word

The following bits describe the receive mode code descriptor Control word. Information contained in this word assists the EXC-1553VME/MCH in message processing. The descriptor control word is initialized by the host and updated by the EXC-1553VME/MCH during command post-processing.

Note: In MIL-STD-1553A, all mode codes are without data, and the T/R bit is ignored.

Bit	Name	Description
15-8	INDX	Index Field. These bits define a multiple message buffer length. The host uses this field to instruct the EXC-1553VME/MCH to buffer "N" messages. "N" can range from 0(00 H) to 256(FF H). If buffer ping-ponging is enabled, the INDX field is "don't care" (i.e., does not contain applicable information). The EXC-1553VME/MCH does not perform message buffering in the ping-pong mode of operation. The index decrements each time a complete message is transacted (no message errors). The index does not decrement if the mode code is illegalized. The EXC-1553VME/MCH can generate an interrupt when the index field transitions from one to zero (see bit 7).
7	INTX	Interrupt Index Equals Zero. Assertion of this bit enables the generation of an interrupt when the index field transitions from one to zero. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. An interrupt is generated after message processing.
6	IWA	Interrupt When Accessed. Assertion of this bit enables the generation of an interrupt when a mode code command is received. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. An interrupt is generated after message processing.
5	IBRD	Interrupt Broadcast Received. Assertion of this bit enables the generation of an interrupt when a valid broadcast mode code command is received. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. An interrupt is generated after message processing.

Bit	Name	Description
4	BAC	Block Accessed. The user initializes this bit to zero; the EXC-1553VME/MCH overwrites the zero with a logic one upon completion of message processing. After interrogating this bit, the user resets this bit to zero to observe further accesses.
3	reserved	Should be set to '0'.
2	A/B	Buffer A/B. Indicates the last buffer accessed when buffer ping-ponging is enabled. During initialization, the user designates the first buffer used by asserting or negating this bit. A logic one indicates buffer A, a logic zero indicates buffer B. This bit is a "don't care" if buffer ping-ponging is not enabled.
1	BRD	Broadcast Received. Assertion of this bit indicates the reception of a valid broadcast command.
0	NII	Notice II. Asserting this bit enables the use of the Broadcast Data Pointer as a buffer for broadcast command information. When negated, broadcast information is stored in the same buffer as non-broadcast information.

6.2.2.4 Mode Code Transmit Control Word

The following bits describe the transmit mode code descriptor Control word. Information contained in this word assists the EXC-1553VME/MCH in message processing. The descriptor control word is initialized by the user and updated by the EXC-1553VME/MCH during command post-processing.

Note: In MIL-STD-1553A, all mode codes are without data, and the T/R bit is ignored.

Bit	Name	Description
15-7	reserved	Should be set to '0'.
6	IWA	Interrupt When Accessed. Assertion of this bit enables the generation of an interrupt when a mode code command is received. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. An interrupt is generated after message processing.
5	IBRD	Interrupt Broadcast Received. Assertion of this bit enables the generation of an interrupt when a broadcast mode code is received. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. An interrupt is generated after message processing.

Bit	Name	Description
4	BAC	Block Accessed. The user initializes this bit to zero; the EXC-1553VME/MCH overwrites the zero with a logic one upon completion of message processing. After interrogating this bit, the host resets this bit to zero to observe further accesses.
3	reserved	Should be set to '0'.
2	A/B	Buffer A/B. This bit indicates the last buffer accessed when buffer ping-ponging is enabled. During initialization, the user designates the first buffer used by asserting or negating this bit. A logic one indicates buffer A; a logic zero indicates buffer B. This bit is a "don't care" if buffer ping-ponging is not enabled.
1	BRD	Broadcast Received. Assertion of this bit indicates the reception of a broadcast command.
0	reserved	Should be set to '0'.

6.2.2.5 Data Pointer A and B (Mode #0)

Data List Pointer A and B contain address information for the retrieval and storage of message data words. In the index mode of operation, the EXC-1553VME/MCH reads Data Pointer A to determine the location of data for retrieval or storage. The EXC-1553VME/MCH uses the Data Pointer to initialize an internal counter; the counter increments after each data word. For a receive command, the EXC-1553VME/MCH stores the incoming data word sequentially into memory. As part of command post-processing, the EXC-1553VME/MCH writes a new data pointer into the descriptor block. The EXC-1553VME/MCH continues to update the data pointer until the Control Word index field decrements to zero. An example is shown in figure 15.

Note: The index feature is not applicable for transmit commands (i.e., T/R bit = 1).

For ping-pong buffer operation, the host uses either Data Pointer A or Data Pointer B. The EXC-1553VME/MCH determines which pointer to access via the state of Control Word bit 2. The EXC-1553VME/MCH retrieves or stores data words from the address contained in the data pointer, automatically incrementing the data pointer as data words are received. The data pointer is never updated as part of command post-processing in the ping-pong mode of operation. See figures 16 and 17.

Bit	Name	Description
15-0	DP[15-0]	Data Pointer Bits. The second and third words of the descriptor block contain the data buffer location. The EXC-1553VME/MCH accesses either Data Pointer A or Data Pointer B depending on the state of Control Word Bit 2 during ping-pong operation. For index operation, the EXC-1553VME/MCH accesses only Data Pointer A. The EXC-1553VME/MCH updates data pointer A after message processing is complete and the index field is not equal to zero and ping-pong operation disabled.

6.2.2.5.1 Ping-Pong Handshake (Mode #0)

The EXC-1553VME/MCH provides a software handshake which indicates the enable and disable of buffer ping-pong operation. During remote terminal operation the EXC-1553VME/MCH asynchronous ping-pongs between two subaddress or mode code data buffers. To perform buffer service, the application software must freeze the remote terminal's access to a single buffer. The EXC-1553VME/MCH's ping-pong enable/disable handshake allows the application software to asynchronously freeze (i.e., disable ping-pong operation) the remote terminal to a single buffer.

The handshake mechanism functions as follows.

Prior to starting remote terminal operation, enable the buffer ping-pong feature by writing a logical 1 to bit 2 of the Control Register. During ping-pong operation, the remote terminal ping-pongs between the two data buffers, for each subaddress or mode code, on a message by message basis. Each unique MIL-STD-1553 subaddress and mode code is assigned two data buffer locations (A and B). The remote terminal retrieves data from a buffer or stores data into a buffer depending on the message type (i.e., transmit or receive command). During ping-pong operation, the remote terminal determines the active subaddress or mode code buffer at the beginning of message processing, the remote terminal complements bit 2 of the Descriptor Control Word to access the alternate buffer on the following message (i.e., ping-pong).

To off-load or load the subaddress and mode code buffers without collisions (e.g., remote terminal writing and application software reading the same buffer), the application software must disable ping-pong operation (i.e., freeze the remote terminal access to a single buffer, either A or B). Disabling ping-pong operation allows the application software to off-load or load the alternate buffer while the remote terminal continues to use the active buffer. To implement this architecture, ping-pong operation must enable and disable asynchronously via software with feedback to indicate that buffer ping-ponging is truly disabled. Second, unique subaddress and mode code flags indicate which buffer is active. Each unique subaddress and mode code is assigned a flag which indicates the active buffer.

To begin the process of off-loading or loading the remote terminal's subaddress and/or mode code buffers, when using the ping-pong feature, the application software performs the following sequences disables ping-pong operation, determines the active buffer, service the alternate buffer, enables ping-pong operation.

The application software disables ping-pong operation by writing a logical zero to Control Register bit 2. The disable of ping-pong operation is acknowledged by bit 9 of the Control Register. Bit 9 of the Control Register acknowledges the ping-pong disable by transitioning from a logical one to a logical zero. The application software interrogates bit 2 of each Descriptor Control Word to determine the active buffer on a subaddress or mode code basis. If bit 2 is a logical zero, the remote terminal uses Buffer A and the application software off-loads or loads Buffer A.

The application software enables ping-pong operation by writing a logical one to Control Register bit 2. The enable of ping-pong operation is acknowledged by bit 9 of the Control Register. Bit 9 of the Control Register acknowledges the ping-pong enable by transitioning from a logical zero to a logical one.

	Data Word #3	021A (H)	Index decrements to 0 (Data Pointer A updated to 010E(H),interrupt generated if enabled)
	Data Word #2	0218 (H)	
	Data Word #1	0216 (H)	
	Time-Tag	0214 (H)	
Command #3 Receive 3 words	Message Info Word	0212 (H)	Index equals 1
	Data Word #2	0210 (H)	Index decrements to 1
	Data Word #1	020E (H)	
	Time-Tag	020C (H)	
Command #2 Receive 2 words	Message Info Word	020A (H)	Index equals 2
	Data Word #3	0208 (H)	Index decrements to 2
	Data Word #2	0206 (H)	
	Data Word #1	0204 (H)	
	Time-Tag	0202 (H)	
Command #1 Receive 3 words	Message Info Word	0200 (H)	Index equals 3

	BROADCAST DATA POINTER	Broadcast Data Pointer: XXXX(H)
	DATA POINTER B	Data Pointer B: XXXX (H)
	DATA POINTER A	Data Pointer A: 0100 (H)
Receive Subaddr #1 Descriptor Block	CONTROL WORD	Index field contents: 03XX (H)

Figure 15. RT Non-Broadcast Receive Message Indexing

Note: X = "don't care"

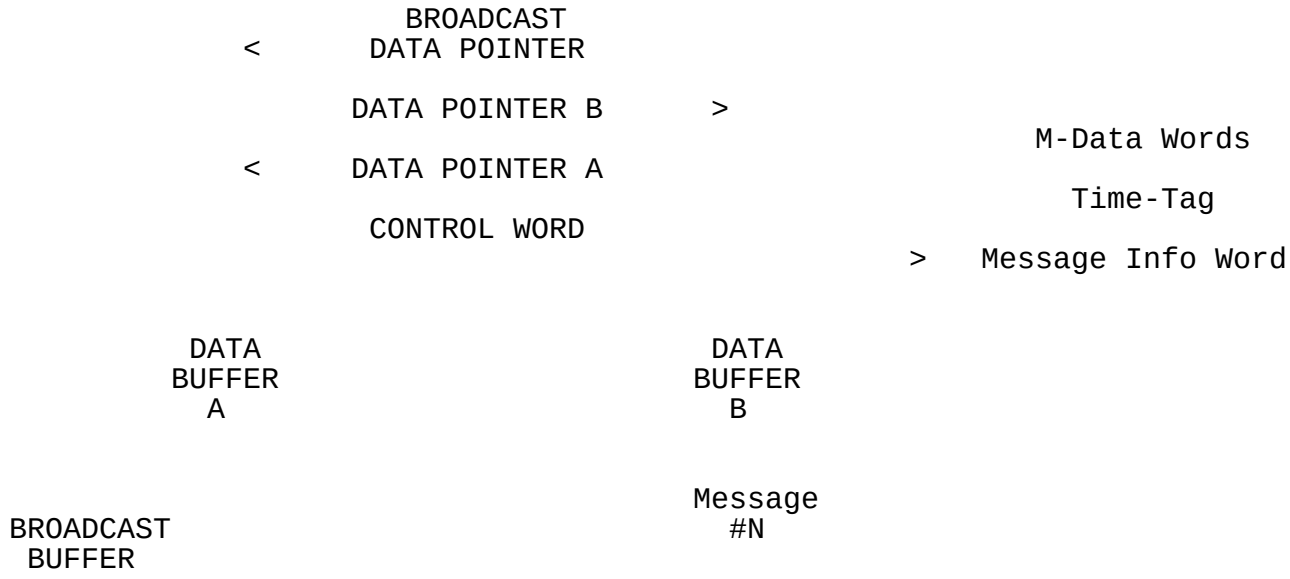


Figure 16. RT Descriptor Block (Receive)

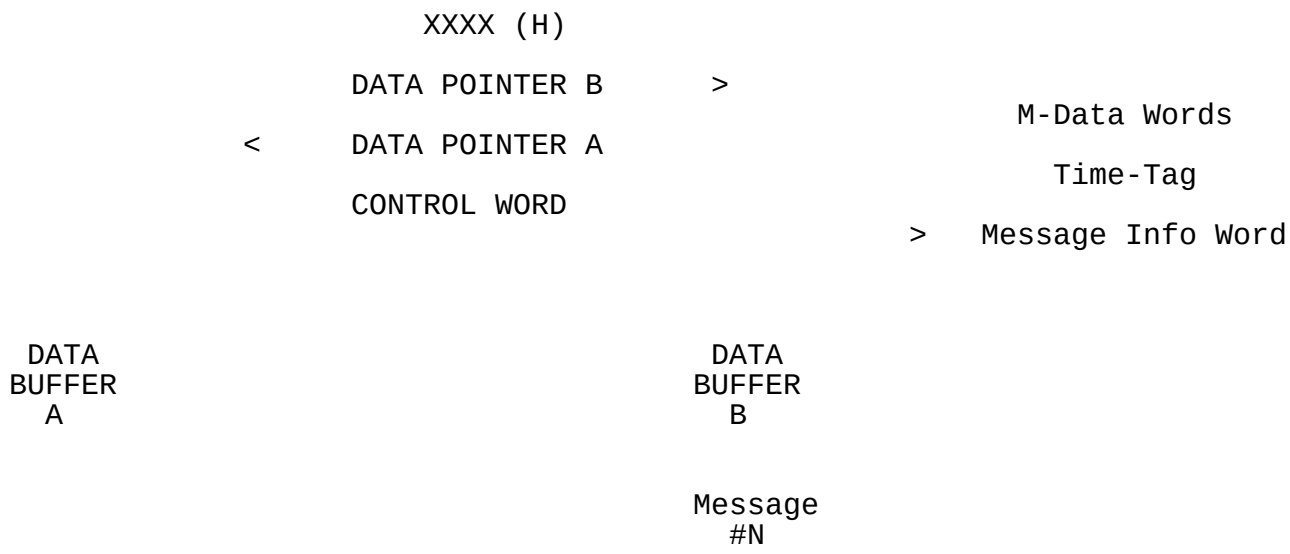


Figure 17. RT Descriptor Block (Transmit)

RT Mode

6.2.2.6 Broadcast Data Pointer (Mode #0)

The following bits describe the receive subaddress/mode code descriptor Broadcast Data Pointer. This word contains the address for the Message Information word, Time-Tag word, and data words associated with a broadcast command. The EXC-1553VME/MCH automatically increments this data pointer during command post-processing, if the ping-pong operation is disabled.

Bit	Name	Description
15-0	BP[15-0]	Broadcast Data Pointer. The fourth word of the descriptor block contains the broadcast data buffer location. This pointer can reside anywhere in memory space. The EXC-1553VME/MCH accesses this pointer when Control Word bit 0 is a logic one and broadcast is enabled. Note 1: If ping-pong is enabled, this pointer does not update. Note 2: When the broadcast command is followed by a Transmit Last Command or Last Status Word mode code, the EXC-1553VME/MCH transmits a status word with bit-time 15 of the 1553 status word set to a logic one. The broadcast bit is cleared by reception of the next valid non-broadcast command.

6.2.3 Data Structures

The following sections discuss the data structures that result from command processing. For each complete message processed, the EXC-1553VME/MCH generates a Message Information word and Time-Tag word. These words aid the host in further message processing. The Message Information word contains word count, message type, and message error information. The Time-Tag word is a 16-bit word containing the command validity time. The Time-Tag word data comes from the EXC-1553VME/MCH's internal Time-Tag counter.

6.2.3.1 Subaddress Receive Data

For receive commands, the EXC-1553VME/MCH stores data words plus two additional words. The EXC-1553VME/MCH adds a Receive Information word and Time-Tag word to each receive command data packet. The EXC-1553VME/MCH places the Receive Information word and Time-Tag word ahead of the data words associated with a receive command (see figures 15, 16, and 17). When message errors occur, the EXC-1553VME/MCH enters the Receive Information word, and Time-Tag word. Once a message error condition is observed, all data words are considered invalid.

Data storage occurs at the memory location pointed to by the data pointer plus two 16-bit locations.

6.2.3.1.1 Receive Information (Info) Word

The following bits describe the Receive Information Word contents.

Bit	Name	Description
15-11	WC[4-0]	Word Count Bits. These five bits contain word count information extracted from the receive command word bit-times 15 to 19.
10	reserved	Ignore on read.
9	BUA/B	Bus A/B. Assertion of this bit indicates that the message was received on bus A. Conversely, if this bit is set to logic zero, the message was received on bus B.
8	RTRT	Remote Terminal to Remote Terminal Transfer. The command processed was an RT-to-RT transfer.
7	ME	Message Error. Assertion of this bit indicates a message error condition was observed during processing. See bits 0 to 4 for details.
6-5	reserved	Ignore on read.
4	ILL	Illegal Command Received. Assertion of this bit indicates the command received was an illegal command.
3	TO	Time-Out Error. Assertion of this bit indicates the EXC-1553VME/MCH did not receive the proper number of data words, i.e., the number of data words received was less than the word count specified in the command word.
2	OVR	Overrun Error. Assertion of this bit indicates the EXC-1553VME/MCH received a word when none was expected or the number of data words received was greater then expected.
1	PRTY	Parity Error. Assertion of this bit indicates the EXC-1553VME/MCH observed a parity error in the incoming data words.
0	MAN	Manchester Error. Assertion of this bit indicates the EXC-1553VME/MCH observed a Manchester error in the incoming data words.

6.2.3.2 Subaddress Transmit Data

The user is responsible for organization of the data packet (i.e., M data words) into memory and establishing the applicable data pointer. The user allocates two memory locations at the top of the data packet for the storage of the Transmit Information word and Time-Tag word. An example transmit data structure for three words is shown below.

```
Data Pointer A --->  @0200 (H)  XXXX    ;reserved for Transmit Info word
equals 0100 (H) @0202 (H)  XXXX    ;reserved for Time-Tag word
                     @0204 (H)  FFFF    ;data word #1
                     @0206 (H)  FFFF    ;data word #2
                     @0208 (H)  FFFF    ;data word #3
```

Note: Data Pointer A points to the top of the data structure not to the top of the data words.

6.2.3.2.1 Transmit Information (Info) Word

The following bits describe the Transmit Information word contents.

Bit	Name	Description
15-11	WC[4-0]	Word Count Bits. These five bits contain word count information extracted from the receive command word bit-times 15 to 19.
10	reserved	Ignore on read.
9	BUA/B	Bus A/B. Assertion of this bit indicates that the message was received on the A bus. Conversely, if this bit is set to logic zero, the message was received on the B bus.
8	reserved	Ignore on read.
7	ME	Message Error. Assertion of this bit indicates a message error condition was observed during processing. See bits 0 to 4 for more detail.
6-5	reserved	Ignore on read.
4	ILL	Illegal Command Received. Assertion of this bit indicates the command received was an illegal command.
3	reserved	Ignore on read.
2	OVR	Overrun Error. Assertion of this bit indicates the EXC-1553VME/MCH received a data word with a Transmit Command.
1-0	reserved	Ignore on read.

6.2.3.3 Mode Code Data

The transmit and receive data structures for mode codes are similar to those for subaddress. The receive data structure contains an Information word, Time-Tag word, and message data word. All receive mode codes with data have one associated data word. Data storage occurs at the memory location pointed to by the data pointer plus two locations. Reception of the synchronize with data mode code automatically loads the Time-Tag counter and stores the data word at the address defined by the data pointer plus two locations.

The transmit mode code data structure contains an Information word, Time-Tag word, and associated data word. The host is responsible for linking the EXC-1553VME/MCH Data Pointer to the data (e.g., Transmit Vector word). For mode codes with internally generated data words (e.g., Transmit BIT word, Transmit Last Command), the transmitted data word is added to the data structure.

For MIL-STD-1553A mode of operation, all mode codes are defined without data words. For mode codes without data, the data structure contains the Message Information word and Time-Tag word only.

Note: In MIL-STD-1553A, all mode codes are without data and the T/R bit is ignored. See section MIL-STD-1553A Operation in following.

6.2.3.3.1 Mode Code Receive Information (Info) Word

The following bits describe the Mode Code Receive Information word contents.

Bit	Name	Description
15-11	MC[4-0]	Mode Code. These five bits contain the mode code information extracted from the receive command word bit-times 15 to 19.
10	reserved	Ignore on read.
9	BUA/B	Bus A/B. Assertion of this bit indicates that the message was received on bus A. Conversely, if this bit is set to logic zero, the message was received on bus B.
8	RTRT	Remote Terminal to Remote Terminal Transfer. Assertion of this bit indicates the command processed was an RT-to-RT transfer.
7	ME	Message Error. Assertion of this bit indicates a message error condition was observed during processing. See bits 0 to 4 for details.
6-5	reserved	Ignore on read.
4	ILL	Illegal Command Received. Assertion of this bit indicates the command received was an illegal command.

Bit	Name	Description
3	TO	Time-out Error. Assertion of this bit indicates the EXC-1553VME/MCH did not receive the proper number of data words, i.e., the number of data words received was less than the word count specified in the command word.
2	OVR	Overrun Error. Assertion of this bit indicates the EXC-1553VME/MCH received a word when none was expected, or the number of data words received was greater than expected.
1	PRTY	Parity Error. Assertion of this bit indicates the EXC-1553VME/MCH observed a parity error in the incoming data words.
0	MAN	Manchester Error. Assertion of this bit indicates the EXC-1553VME/MCH observed a Manchester error in the incoming data words.

6.2.3.3.2 Mode Code Transmit Information (Info) Word

The following bits describe the Mode Code Transmit Information word contents.

Bit	Name	Description
15-11	MC[4-0]	Mode Code. These five bits contain the mode code information extracted from the command word bit-times 15 to 19.
10	reserved	Ignore on read.
9	BUA/B	Bus A/B. Assertion of this bit indicates that the message was received on bus A. Conversely, if this bit is set to logic zero, the message was received on bus B.
8	reserved	Ignore on read.
7	ME	Message Error. Assertion of this bit indicates a message error condition was observed during processing. See bits 0 to 4 for details.
6-5	reserved	Ignore on read.
4	ILL	Illegal Command Received. Assertion of this bit indicates the command received was an illegal command.
3	reserved	Ignore on read.
2	OVR	Overrun Error. Assertion of this bit indicates the EXC-1553VME/MCH received a data word with a Transmit Command.
1-0	reserved	Ignore on read.

6.2.4 RT Circular Buffer Modes #1 and #2

The RT circular buffer modes simplify the software service of remote terminals implementing bulk or periodic data transfers. The user selects the preferred mode, at start-up by writing to Control Register bits 7 and 8 (see Control Register above). The two modes (Mode #1 and Mode #2) are discussed in following paragraphs.

6.2.4.1 Mode #1 Operation

In this mode the EXC-1553VME/MCH merges transmit or receive data into a circular buffer along with message information.
For each valid receive message, the EXC-1553VME/MCH enters a message information word, time-tag word, and data word(s) into a unique receive circular buffer.
For each valid transmit message, the EXC-1553VME/MCH enters a message information word and time-tag word into reserved memory locations within the transmit circular buffer. The EXC-1553VME/MCH automatically controls the wrap around of circular buffers.

6.2.4.1.1 Mode #1 Descriptor Block

Each subaddress and mode code, both transmit and receive, has a unique circular buffer assignment. The EXC-1553VME/MCH decodes the command word T/R bit, subaddres/mode code field, and word_count/mode_code field to select a unique descriptor block which contains Control Word, TA, CA, and BA (see figure 18).

To implement Circular Buffer 1's architecture, the four word descriptor block and Control Register are different than in the Mode #0. Bits 15 through 8 of the Control Word are don't care. The second word of the descriptor block defines the buffer's starting or top address (TA). The TA pointer remains static during message processing . The fourth entry into the descriptor block identifies the buffer's bottom address (i.e., BA) and also remaines static during message processing. The third descriptor block words represent the current address (i.e., CA) in the buffer and is dynamic. If the EXC-1553VME/MCH observes no message error conditions, the CA pointer updates at the end of message processing. The application software reads the dynamic CA pointer to determine the current bottom of the buffer.

The TA (top of buffer) and BA (bottom of buffer) pointers define the circular buffer's length. The CA pointer identifies the current address (i.e., last accessed address plus one). The circular buffer wraps to the top address after completing a message that results in CA being greater than or equal to BA. If CA increments past BA during intra-message processing, the EXC-1553VME/MCH will access memory (read or write) address locations past BA. Delimit all circular buffer boundaries with at least 34 address locations.

Note: In this mode of operation, bits INDX, NII and A/B of the descriptor Control Word and the PPEN bit of the Control Register are don't care.

6.2.4.1.2 Mode #1 Circular Buffer

First, a review of receive message processing. The EXC-1553VME/MCH begins all message processing by reading a unique descriptor block after reception and validation of a subaddress or mode code command word. The EXC-1553VME/MCH internally increments the CA pointer to store the receive data word(s). After message processing completes, the EXC-1553VME/MCH stores the message information word and time-tag word into the circular buffer preceding the message data. At the end of message processing, the EXC-1553VME/MCH updates CA (if no errors detected). For CA larger than BA storage of next message begins at the address location pointed to by the TA pointer, and CA is made equal to TA. If CA is less than BA, CA points to the next available memory location in the buffer (i.e., CA+1).

For transmit commands, the EXC-1553VME/MCH begins transmission of data from memory location CA+2. Reserve the first two locations for the message information word and time-tag word. After message processing completes, the EXC-1553VME/MCH enters the message information word and time-tag word into the circular buffer. At the end of message processing, the EXC-1553VME/MCH updates CA (if no errors detected). For CA larger than BA, storage of the next message begins at the address location pointed to by the TA pointer, and CA is made to equal TA. If CA is less than BA, CA points to the next available memory location in the buffer (i.e., CA+1).

Note: In this mode the Message Information word bit 5 reflects the reception of broadcast message via the BRD bit.

The EXC-1553VME/MCH generates a circular buffer empty/full interrupt when the buffer reaches the end (i.e., CA greater than BA) and begins a new message at the top of the buffer. Bit 8 of the Mask Register and bit 7 of the Descriptor Control Word mask enables the generation of the Full/Empty interrupt.

Figure 18 describes the relationship between TA, BA, and CA.

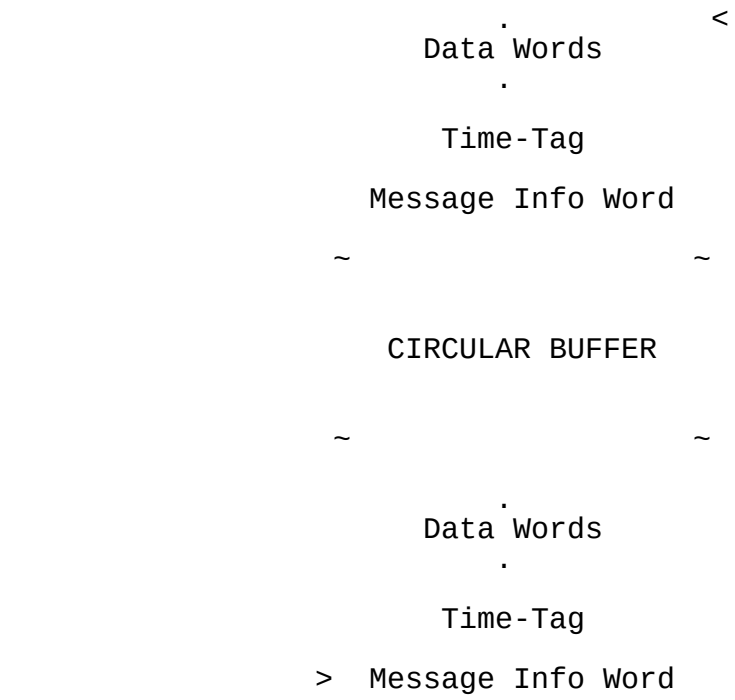


Figure 18. RT Mode #1 Descriptor Block and Circular Buffer

6.2.4.2 Mode #2 Operation

In this mode the EXC-1553VME/MCH separates message data and message information into unique circular buffers. The separation of data from message information simplifies the software that loads and unloads data from the buffers. The message information buffer contains Time-Tag and Mesage Information words for each message trasnacted on the bus, while the data buffer contains the message data words. Both buffers wrap-around after processing a pre-determined number of messages.

6.2.4.2.1 Mode #2 Descriptor Block

Each subaddress and mode code, both trasmit and receive, has a unique pair of circular buffers. The EXC-1553VME/MCH decodes the command word T/R bit, subaddres/mode field, and word_count/mode_code field to select a unique descriptor block which contains Control Word, TA, CA, and MIB (see figure 19).

To implement Circular Buffer 2's architecture, the descriptor block and Control Register are different than in Mode #0. Bits 15 through 8 of the Control Word specify the Message Information Buffer (MIB) length; the maximum MIB size is 256. Table 3 shows how the Control Word's most significant bits select the depth of the MIB. The Control Words eight most significant bits remain static during message processing.

The second word of the description block defines the top address (TA) of the data circular buffer. The TA pointer remains static during message processing. The third descriptor word identifies the current address (i.e., CA) of the data circular buffer. The application software reads the dynamic CA pointer to determine the current address of the data buffer. The EXC-1553VME/MCH increments the CA pointer, at the end of message processing, until the MIB buffer is full. When the MIB wraps around, the SuMMIT loads the CA pointer with the TA pointer.

The fourth word in the descriptor block defines the top or base address of the Message Information Buffer (i.e., MIB) and the current MIB address (i.e., offset from base address). The SuMMIT enters the message information word and time-tag word into the MIB, for each message, until the end of the MIB is reached. When the MIB reaches the end, the next message's message information word and time-tag word is entered at the top of the MIB. The MIB pointer is a semi-static pointer. The EXC-1553VME/MCH updates the current address field at the end of message processing. The base address field remains static.

Note: In this mode of operation, bits INDX, NII and A/B of the descriptor Control Word and the PPEN bit of the Control Register are don't care.

6.2.4.2.2 Mode #2 Circular Buffer

First is a review of receive message processing. The EXC-1553VME/MCH begins all message processing by reading the descriptor block of the subaddress or mode code command received (i.e., Control Word, TA, CA, and MIB). The EXC-1553VME/MCH begins storage of data word(s) starting at the location contained in the CA pointer. The EXC-1553VME/MCH automatically updates the CA pointer internally as message processing progresses. After receiving the correct number of data words, the EXC-1553VME/MCH stores the message information word and time-tag word into the MIB. At the end of message processing, the EXC-1553VME/MCH updates CA and the MIB Current Address Field (CAF). If CAF equals the specified MIB length, CA is updated to TA and the MIB CAF is reset to zero. If CAF is less than the specified MIB length, CA and MIB CAF point to the next available memory location in each buffer. Control Word bits 15 to 8 specify the MIB length.

For transmit commands, the EXC-1553VME/MCH begins transmission of data from memory location CA. After message processing completes, the EXC-1553VME/MCH enters the message information word and time-tag word into the MIB. At the end of message processing, the EXC-1553VME/MCH updates CA and the MIB CAF. If CAF equals the specified MIB length, CA is updated to TA and the MIB CAF is reset to zero. If CAF is less than the specified MIB length, CA and MIB CAF point to the next available memory location in each buffer.

Note: In this mode the BRD bit is added to the Message Information word bit 5.

The EXC-1553VME/MCH generates a circular buffer empty/full interrupt when the MIB reaches the end and begins a new message at the top of the buffer. Bit 8 of the Mask Register and bit 7 of the descriptor Control Word mask and enable the generation of the Full/Empty interrupt.

Figure 19 describes the relationship between TA, CA, and MIB.

Control Word Bits 15-8	Length of MIB (messages)	MIB Pointer Structure (Base and CAF)
FF	128	8 Bit Base Address +8 Bit Current Address Field
7F	64	9 Bit Base Address +7 Bit Current Address Field
3F	32	10 Bit Base Address +6 Bit Current Address Field
1F	16	11 Bit Base Address +5 Bit Current Address Field
0F	8	12 Bit Base Address +4 Bit Current Address Field
07	4	13 Bit Base Address +3 Bit Current Address Field
03	2	14 Bit Base Address +2 Bit Current Address Field
01	1	15 Bit Base Address +1 Bit Current Address Field

Table 3. RT Mode #2 Control Word and MIB Pointer Structure

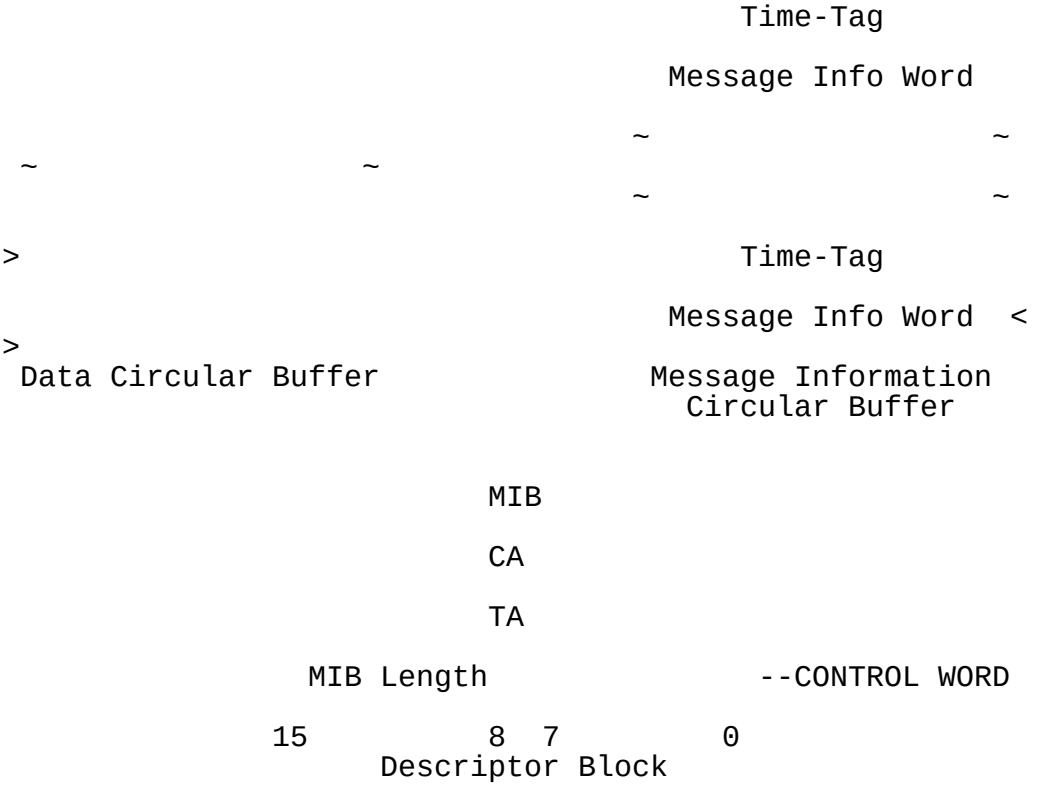


Figure 19. RT Mode #2 Descriptor Block and Circular Buffers

6.2.5 Mode Code and Subaddress

The EXC-1553VME/MCH provides subaddress and mode code decoding that meets MIL-STD-1553B requirements. In addition, the EXC-1553VME/MCH has automatic internal illegal command decoding for reserved MIL-STD-1553B mode codes. Table 4 shows the EXC-1553VME/MCH's response to all possible mode code combinations.

Table 4. RT Mode Code Description

T/R	Mode Code	Function	Operation
0	00000-01111	Undefined (w/o data)	1. Command word stored 2. Status word transmitted
0	10000	Undefined (with data)	1. Command word stored 2. Data word stored 3. Status word transmitted
0	10001	Synchronize (with data)	1. Command Word stored 2. Data word stored 3. Time-Tag counter loaded with data word value 4. Status word transmitted
0	10010	Undefined	1. Command word stored 2. Data word stored 3. Status word transmitted
0	10011	Undefined	1. Command word stored 2. Data word stored 3. Status word transmitted
0	10100	Selected Transmitter	1. Command word stored

		Shutdown	2. Data word stored 3. Status word transmitted
0	10101	Override Selected Transmitted Shutdown	1. Command word stored 2. Data word stored 3. Status word transmitted
0	10110-11111	Reserved	1. Command word stored 2. Data word stored 3. Status word transmitted
1	00000	Dynamic Bus Control	1. Command word stored 2. Dynamic Bus Acceptance set in outgoing status if enabled in the Register 3. Status word transmitted
1	00001	Synchronize	1. Command word stored 2. Time-Tag counter reset 0000 (H) 3. Status word transmitted
1	00010	Transmit Status Word	1. Command word stored 2. Last status word 3. Status word cleared Note: EXC-1553VME/MCH status word if illegalized

bit word Control

to

transmitted after master reset

updates

RT Mode

T/R	Mode Code	Function	Operation
1	00011	Initiate Self-Test	1. Command word stored 2. Status word transmitted 3. B.I.T. initiated 4. TF bit set if BITF bit asserted
1	00100	Transmitter Shutdown	1. Command word stored 2. Status word transmitted 3. Alternate bus disabled
1	00101	Override Transmitter Shutdown	1. Command word stored 2. Status word transmitted 3. Alternate bus enabled Note: Reception of the transmitter shutdown code does not enable bus not previously bled in the Control ister. Reset remote minal mode code the transmitter shutdown function.
1	00110	Inhibit Terminal Flag Bit	1. Command word stored 2. Terminal flag bit set zero and assertion

override mode a ena- Reg- ter- clears shutdown

to disabled

RT Mode

			3. Status word transmitted
1	00111	Override Inhibit Terminal Flag enabled	1. Command Word stored 2. Terminal flag bit for assertion 3. Status word transmitted
1	01000	Reset Remote Terminal	1. Command word stored 2. Status word transmitted 3. RT Mode reset, see Reset for more information on software reset section
1	01001-01111	Reserved	1. Command word stored 2. Status word transmitted
1	10000	Transmit Vector Word to the outgoing	1. Command word stored 2. Service request bit set a logic zero in status 3. Status word transmitted 4. Data word transmitted 5. Clears the SRQ bit in 1553 Status Word Bits Register
1	10001	Reserved	1. Command word stored 2. Status word transmitted 3. Data word transmitted

T/R	Mode Code	Function	Operation
1	10010	Transmit Last Command	1. Command word not stored 2. Last status word transmitted 3. Last command word transmi-tted 4. Data word stored (Transmit Last Command) 5. Transmitted data word is all zero after reset Note: The RT Mode stores the Transmit Last Command mode code if illegalized and updates status word
1	10011	Transmit BIT Word	1. Command word stored 2. Status word transmitted 3. BIT word transmitted from BIT Word Register 4. Data word stored (Transmit BIT Word)
1	10100-10101	Undefined (with data)	1. Command word stored 2. Status word transmitted 3. Data word transmitted
1	10110-11111	Reserved	1. Command word stored 2. Status word transmitted

6.2.6 Encoder and Decoder

The EXC-1553VME/MCH receives the command word from the MIL-STD-1553 bus and processes it either by the primary or secondary decoder. Each decoder checks for the proper sync pulse and Manchester waveform, edge skew, correct number of bits, and parity. If the command is a receive command, the EXC-1553VME/MCH processes each incoming data word for correct format, word count, and contiguous data. If a message error is detected, the EXC-1553VME/MCH stops processing the remainder (if any) of the message, suppresses status word transmission, and asserts bit-time 9 (ME bit) of the status word.

The EXC-1553VME/MCH automatically compares the transmitted word (encoder word) to the reflected decoder word by way of the continuous loop-back feature. If the encoder word and reflected word do not match, the WRAPF bit is asserted in the BIT Word Register. In addition to the loop-back compare test, a timer precludes a transmission greater than 800 usec by the assertion of Fail-Safe Timer. This timer is reset upon receipt of another command. Remote Terminal Response-Time:

MIL-STD-1553A = 7 usec
MIL-STD-1553B = 10 usec
Data Contiguity Time-Out = 1.0 usec

6.2.7 RT-RT Transfer Compare

The RT-to-RT Terminal Address compare logic ensures that the incoming status word's Terminal Address matches the Terminal Address of the transmitting RT specified in the command word. An incorrect match results in setting the message-error bit and suppressing transmission of the status word. (RT-to-RT transfer time-out = 55 to 59 usec). The EXC-1553VME/MCH does not check ME or SSYSF of the transmitting remote terminal when receiving.

6.2.8 Terminal Address

The EXC-1553VME/MCH Terminal Address is programmed via the most significant six bits in the Operational Status Register: RTA[4-0] and RTAPTY. The Terminal Address parity is odd; RTAPTY is set to a logic state to satisfy this requirement. Assertion of Operational Status Register bit 2 (TPARF) indicates incorrect Terminal Address parity.

For example:

RTA[4-0] = 05(H) = 00101
RTAPTY = 1(H) = 1
Sum of 1s = 3(odd), Operational Status Reg. Bit 2 = 0

RTA[4-0] = 04(H) = 00100
RTAPTY = 0(H) = 0
Sum of 1s = 1(odd), Operational Status Reg. Bit 2 = 0

RTA[4-0] = 04(H) = 00100
RTAPTY = 1(H) = 1
Sum of 1s = 2(even), Operational Status Reg. Bit 2 = 1

Notes:
-The EXC-1553VME/MCH checks the Terminal Address and parity after RT mode operation has been started. With Broadcast disabled, RTA[4-0] = 11111 operates as a normal RT address.
-The BIT Word Register parity fail bit is valid after RT mode has been started.

6.2.9 Reset

The software reset (see Channel Reset Register) is also equivalent to a hardware (power-on) reset and takes 5 usec to complete. Assertion of reset results in the immediate reset of the channel and termination of command processing. The user is responsible for the re-initialization of the RT Mode for operation.

A Reset Remote Terminal mode code (Mode Code 01000, T/R = 1) clears the encoder/decoders, resets the time-tag, enables the busses to the programmed host state, and re-enables the Terminal Flag for assertion. This reset is performed after the transmission of the 1553 Status word.

6.2.10 MIL-STD-1553A Operation

To maximize flexibility, the EXC-1553VME/MCH can operate in many different systems which use various protocols. Specifically, two of the protocols that the EXC-1553VME/MCH may be interfaced to are MIL-STD-1553A and MIL-STD-1553B. To meet these protocols, the EXC-1553VME/MCH may be configured through Control Register bits. Table 5 defines the three ways to program the EXC-1553VME/MCH.

Table 5. RT MIL-STD-1553A Operation

A/B_STD	XMTSW	RESULT (protocol selected)
0	X	1553B response, 1553B Standard
1	0	1553A response, 1553A Standard
1	1	1553A response, Auto execute the TRANSMIT LAST STATUS WORD mode code.

When configured as a remote terminal to meet MIL-STD-1553A, the EXC-1553VME/MCH will operate as follows:

- responds with a status word within 7 usec;
- ignores the T/R bit for all mode codes;
- all mode codes are defined without data;
- all mode codes use mode code transmit control and information words;
- mode code 00000 is defined as Dynamic Bus Control (DBC);
- subaddress 00000 defines a mode code;
- ME and TF bits are defined in the 1553 status word; all other status word bits are programmable (i.e., NO BUSY mode,etc.);
- broadcast of all mode codes, except Mode Code 00000 (DBC) and Mode Code 00010 (Transmit Status word if enabled), is allowed.
- to illegalize a Mode Code, the user needs to illegalize both the receive and transmit versions;
- illegalization of row 1F(H) is not automatic;

6.3 BUS MONITOR MODE (BM MODE)

6.3.1 Control Registers for BM Mode

The control registers are read/write unless otherwise stated. All control registers **must** be accessed in word mode. All control register bits are active high and are reset to '0' unless otherwise stated.

reserved	003E (H)
	0020 (H)
MONITOR FILTER LO REG	001E (H)
MONITOR FILTER HI REG	001C (H)
MONITOR BLOCK COUNTER REG	001A (H)
INITIAL MONITOR DATA POINTER REG	0018 (H)
INITIAL MONITOR CMD BLK PTR REG	0016 (H)
reserved	0014 (H)
	0010 (H)
TIME-TAG REG	000E (H)
BIT WORD REG	000C (H)
INTERRUPT LOG LIST POINTER REG	000A (H)
PENDING INTERRUPT REG	0008 (H)
INTERRUPT MASK REG	0006 (H)
CURRENT COMMAND BLOCK REG	0004 (H)
OPERATIONAL STATUS REG	0002 (H)
CONTROL REGISTER	0000 (H)

Figure 20. BM Control Registers Map

6.3.1.0 Description of BM Mode Control Registers

6.3.1.1 Control Register 0000 (H) Read/Write

To operate the EXC-1553VME/MCH as a bus monitor, use the following bits. To make changes to the Bus Monitor and to this register, the STEX bit (Bit 15) must be logic zero.

Note: The user has 5 usec after TERACT (OPERATIONAL STATUS REGISTER bit 0) active to stop execution.

Bit	Name	Description
15	STEX	Start Execution. Assertion of this bit commences operation of the EXC-1553VME/MCH. A Control Register write negating this bit inhibits operation of the EXC-1553VME/MCH. After execution has begun, a write of a logic zero will halt the EXC-1553VME/MCH after completing the current 1553 message.
14	SBIT	Start B.I.T. Assertion of this bit places the channel into the Built-In Test routine. The BIT test takes 1 ms to execute and has a 93.4% fault coverage. If the channel has been started, the host must halt the channel in order to place the channel into the Built-In Test routine (STEX = 0). Note: If Start B.I.T. (SBIT) and Start Execution (STEX) are both set on one register write, BIT has priority.
13-11	reserved	Should be set to '0'.
10	PTCE	Programmable Timer Clock Enable. Assertion of this bit enables a programmable clock used with an internal time-tag counter. Refer to Programmable Timer Clock Register section described above. If set to logic zero, the EXC-1553VME/MCH will use an internal fixed clock. Refer to Time-Tag Register. Note: The user can only change the clock frequency source before starting the EXC-1553VME/MCH (i.e., setting STEX bit to '1').
9	ERTO	Extended Response Time-Out. Assertion of this bit enables the extended response time-out option and forces the BM Mode to look for an RTs response time in 30 usec or generate time-out errors. Negation of this bit enables for the standard time-out in 14 usec.
8-6	reserved	Should be set to '0'.

Bit	Name	Description
5	BMTC	Bus Monitor Control. This bit determines whether the EXC-1553VME/MCH will monitor all RTs or selected RTs. If this bit is set to logic zero, the EXC-1553VME/MCH will monitor all RTs. If this bit is set to logic one, the EXC-1553VME/MCH will monitor only the RTs as specified in the Monitor Filter Hi & Lo Registers.
4	BCEN	Broadcast Enable. This bit, if set to logic one, allows RT address 31 to be used as a Broadcast message. If set to logic zero, then address 31 is a normal address.
3-2	reserved	Should be set to '0'.
1	INTEN	Interrupt Log List Enable. Assertion of this bit enables the Interrupt Log List. Negation of this bit prevents the logging of interrupts as they occur.
0	reserved	Should be set to '0'.

6.3.1.2 Operational Status Register 0002 (H) Read/Write

This register provides pertinent status information for BM Mode and is not reset to 0000H on reset. Instead the bit A/B_STD is set to '1'.

Note: To make changes to the BM and to this register, the STEX bit (Control Register, bit 15) must be logic zero.

Bit	Name	Description
15-10	reserved	Should be set to '0'.
9	MSEL1	Mode Select 1. In conjunction with Mode Select 0, this bit determines the EXC-1553VME/MCH mode of operation.
8	MSEL0	Mode Select 0. In conjunction with Mode Select 1, this bit determines the EXC-1553VME/MCH mode of operation.
7	A/B_STD	Military Standard 1553A or 1553B Standard. This bit determines whether the EXC-1553VME/MCH will look for the RT's response in 7 usec (MIL-STD-1553A) or in 12 usec (MIL-STD-1553B). Assertion of this bit forces the Bus Monitor to declare a time-out error condition if the RT has not responded in 9 usec. Negation of this bit allows the Bus Monitor to declare a time-out error condition if the RT has not responded in 14 usec.
6-5	reserved	These read-only bits should be ignored on read.

MSEL1	MSEL0	Mode of Operation
0	0	BC Mode
0	1	RT Mode
1	0	BM Mode
1	1	RT/ Concurrent BM Mode

Bit	Name	Description
4	reserved	Should be set to '0'.
3	EX	EXC-1553VME/MCH Channel Executing. This read-only bit indicates whether the channel is presently executing or whether it is idle. A logic one indicates that the channel is executing; a logic zero indicates idle.
2	reserved	Should be set to '0'.
1	READY	Channel Ready. This read-only bit indicates that the channel has completed initialization or B.I.T. This bit is cleared on reset.
0	TERACT	Channel Terminal Active. This read-only bit indicates that the channel is presently processing a 1553 message. This bit is cleared on reset.

6.3.1.3 Current Command Register 0004 (H) - READ ONLY

This register contains the last valid command that was transmitted over the 1553 bus. In an RT-RT transfer, this register will update as each of the two commands are received by the Bus Monitor.

Bit	Name	Description
15-0	CC[15-0]	Current Command. These bits contain the latest 1553 command word that was received by the Bus Monitor.

6.3.1.4 Interrupt Mask Register 0006 (H) Read/Write

The EXC-1553VME/MCH interrupt architecture allows the host to mask or temporarily disable the service of interrupts. While masked, interrupt activity does not occur. The unmasking of an interrupt after the event occurs does not generate an interrupt for that event. An interrupt is masked if the corresponding bit of this register is set to logic zero.

Bit	Name	Description
15-12	reserved	Should be set to '0'.
11	MERR	Message Error Interrupt.
10-1	reserved	Should be set to '0'.
0	MBC	Monitor Block Counter Interrupt.

6.3.1.5 Pending Interrupt Register 0008 (H) - READ-ONLY

The pending interrupt register is used to identify which of the interrupts occurred during operation. Note that all register bits are cleared on a host read.

Bit	Name	Description
15-12	reserved	Ignore on read.
11	MERR	Message Error Interrupt. This bit is set if a message error occurs. The Bus Monitor can detect Manchester, sync-field, word count, 1553 word parity, bit count, and protocol errors. This bit will be set and an interrupt generated after message processing is complete.
10-1	reserved	Ignore on read.
0	MBC	Bus Monitor Block Counter Interrupt. This bit is set if the EXC-1553VME/MCH's monitor block counter reaches zero (transition from 1 to 0). It should be noted that the Bus Monitor does not discriminate between error-free messages and those messages with errors.

6.3.1.6 Interrupt Log List Pointer Register 000A (H) Read/Write

This register indicates the starting address of the Interrupt Log List. The Interrupt Log List is a 32-word ring-buffer that contains information pertinent to the service of interrupts. The EXC-1553VME/MCH architecture requires the location of the Interrupt Log List on a 32-word boundary. The most significant 11 bits of this register designate the location of the Interrupt Log List within a 64K memory space. Initialize the lower five-bits of this register to a logic zero. The EXC-1553VME/MCH controls the lower five-bits to implement the ring-buffer architecture. This register is read to determine the location and number of interrupts within the Interrupt Log List (least significant five-bits).

Bit	Name	Description
15-0	ILLP[15-0]	Interrupt Log List Pointer Bits.

Note: Bits 15-5 indicate the starting Base address while bits 4-0 indicate the ring location of the Interrupt Log List.

6.3.1.7 BIT Word Register 000C (H) Read/Write

This register contains information on the current health of the channel's hardware. The lower 8 bits of this register are user-defined.

Bit	Name	Description
15	DMAF	DMA Fail. This bit is set if all channel's internal DMA activity had not been completed within 7 usec.
14-13	reserved	Should be set to '0'.
12	BITF	BIT Fail. Assertion of this bit indicates a B.I.T. failure. Interrogate bits 11 and 10 to determine the specific bus that failed.
11	BUAF	Bus A Fail. Assertion of this bit indicates a B.I.T. failure in Bus A.
10	BUBF	Bus B Fail. Assertion of this bit indicates a B.I.T. failure in Bus B.
9	MSBF	Memory Test Fail. Most significant memory byte failure.
8	LSBF	Memory Test Fail. Least significant memory byte failure.
7-0	UDB[7-0]	User-Defined Bits.

6.3.1.8 Time-Tag Register 000E (H) - READ ONLY

This register reflects the state of a 16-bit free running ring counter in the RT and BM modes. This counter will remain a free running counter as long as the channel is not in a reset mode. This counter may be driven by the Programmable Timer Clock (see PTCE bit within Control Register). If not driven by the Programmable Timer Clock, this counter is clocked by a fixed 15.625 KHz (64 usec) clock. The Time-Tag counter begins operation immediately after reset or within 64 usec.

Bit	Name	Description
15-0	TT[15-0]	Time-Tag Counter Bits. These bits indicate the state of the 16-bit internal counter.

6.3.1.9 Initial Monitor Block Pointer Register 0016 (H) Read/Write

This register contains the starting location of the Monitor Blocks.

Note: It is recommended that this register not be changed while the Bus Monitor mode is active (i.e., Operational Status Register bit EX =1).

Bit	Name	Description
15-0	MBA[15-0]	Initial Monitor Block Address. These bits indicate the starting location of the Monitor Block.

6.3.1.10 Initial Monitor Data Pointer Register 0018 (H) Read/Write

This register contains the starting location of the Monitor Data.

Note: It is recommended that this register not be changed while the Bus Monitor mode active (i.e., Operational Status Register bit EX = 1).

Bit	Name	Description
15-0	MDA[15-0]	Initial Monitor Data Address. These bits indicate the starting location of the Monitor Data.

6.3.1.11 Monitor Block Counter Register 001A (H) Read/Write

This register contains the number of Monitor Blocks the user wishes to log. After execution begins, this register automatically decrements as commands are logged. When this register is decremented from one to zero, an interrupt will be generated, if enabled. The Bus Monitor will start over at the initial pointers as identified in the Initial Monitor Block Pointer Register and the Initial Monitor Data Pointer Register.

Note: It is recommended that this register not be changed while the Bus Monitor is active (i.e., Operational Status Register, bit EX = 1).

Bit	Name	Description
15-0	MBC[15-0]	Monitor Block Count. These bits indicate the number of Monitor Blocks to log.

6.3.1.12 Monitor Filter Hi Register 001C (H) Read/Write

This register determines which RTs (RT 31 through RT 16) the EXC-1553VME/MCH will monitor.

Bit	Name	Description
15-0	MFH[31-16]	Monitor Filter Hi. These bits determine which RT to monitor.

6.3.1.13 Monitor Filter Lo Register 001E (H) Read/Write

This register determines which RTs (RT 15 through RT 0) the EXC-1553VME/MCH will monitor.

Bit	Name	Description
15-0	MFL[15-0]	Monitor Filter Lo. These bits determine which RT to monitor.

6.3.2 Bus Monitor Architecture

To meet the MIL-STD-1553 monitor requirements, the EXC-1553VME/MCH utilizes a Monitor Block architecture that takes advantage of both control registers and RAM. The Monitor Block, which is located in contiguous memory, requires eight locations for each message. These eight locations include a message information word, two command word locations, a data pointer, two status word locations, a time-tag location, and a reserved location.

The user must initialize the starting locations of the Monitor Block, the Data Pointer, Block Counter, and the Interrupt Log Pointer. From then on, the EXC-1553VME/MCH will build a Monitor Block for each message it receives over the 1553 bus. Figure 21 shows a diagram of the Monitor Block followed by a description of each location associated with the Monitor Block.

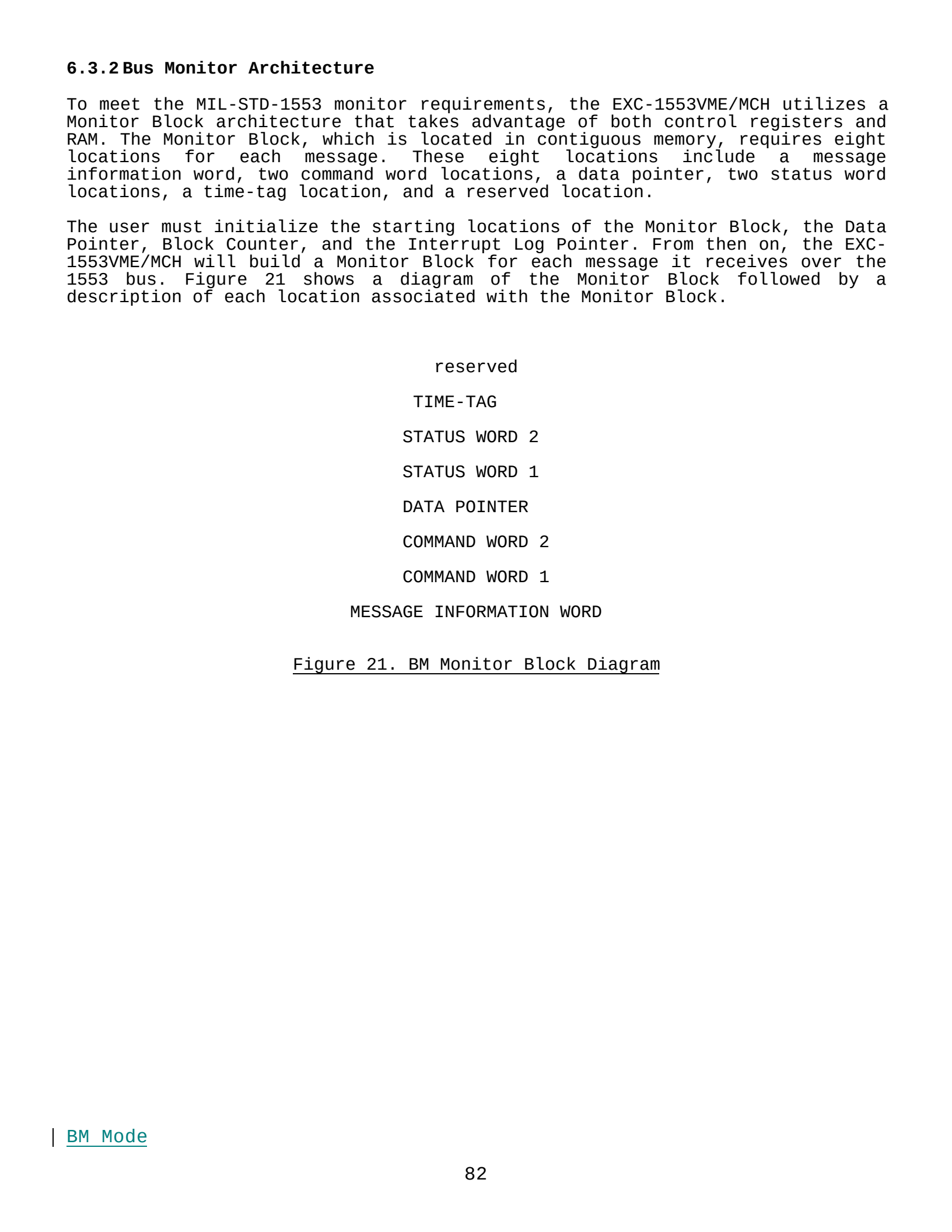
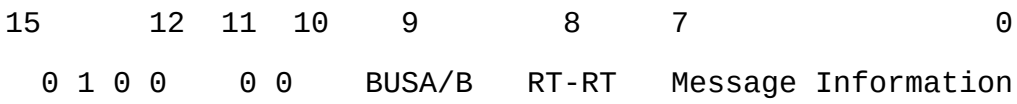


Figure 21. BM Monitor Block Diagram

BM Mode

6.3.2.1 Message Information Word

The first memory location of each Monitor Block contains the message information word. Each message information word contains the opcode, retry number, bus definition, RT-RT messages, and the message information.



Bit Number	Description
15-12	Default. With the Monitor Block architecture resembling the BC Command Block architecture, these bits default to a "0100" state (which is the Execute and Continue opcode) in case the monitor must switch to the BC mode of operation.
11-10	Default. With the Monitor Block architecture resembling the BC, these bits default to a "00" state. If the monitor must switch to the BC, the retries will be set at four per message.
9	Bus A/B. This bit defines on which of the two buses the command was received. (Logic 1 = Bus A, Logic 0 = Bus B).
8	RT-RT Transfer. This bit defines whether or not the message associated with this Monitor Block was an RT-RT transfer and whether the EXC-1553VME/MCH saved the second command word. This bit will be set only if the EXC-1553VME/MCH is instructed to monitor the Receive RT.
7-0	Message Information. These bits define the conditions of the message received by the EXC-1553VME/MCH for that particular Monitor Block. Each of the message information bits is defined in the following section.

6.3.2.1.1 Message Information Bits

Message information bits are provided as a means to supply more data on the message. In an RT-RT transfer, the information applies to the complete message. Each message information bit is defined below.

Bit Number	Description
7	Message Error. This bit will be set if the monitor detects an error in either the command word, data words, or the RT's status.

Bit Number	Description
6	Mode Code without Data. This bit will be set if the monitor detects that the command being processed is a mode code without data words.
5	Broadcast. This bit will be set if the monitor detects that the command being processed is a broadcast message.
4	Reserved.
3	Time-out Error. This bit will be set if the BM did not receive the proper number of data words, e.g., the number of data words received was less than the word count specified in the command word.
2	Overrun Error. This bit will be set if the BM received a word when none were expected or the number of data words received was greater than expected.
1	Parity Error. This bit will be set if a parity error has occurred on one of the message words.
0	Manchester Error. This bit will be set if a Manchester error has occurred on one of the data words.

6.3.2.2 Command Words

The next two locations in the EXC-1553VME/MCH Monitor Block are for command words. In non-RT-RT 1553 messages, only the first command word will be stored. However, in an RT-RT transfer, the first command word is the Receive Command and the second command word is the Transmit Command.

6.3.2.3 Data Pointer

The fourth location in the Monitor Block is the data pointer. This pointer points to the first memory location to store the data words associated with the message for this block. Note that the data associated with each individual message will be stored contiguously. This data structure allows the EXC-1553VME/MCH to store the specified number of data words. (Note: In an RT-RT transfer, the Bus Monitor uses the data pointer as the location in memory to store the transmitting data in the transfer.)

6.3.2.4 Status Words

The next two locations in the Monitor Block are for status words. As the RT responds to the BC's command, the corresponding status word will be stored in Status Word 1. However, in an RT-RT transfer, the first status word will be the status of the Transmitting RT while the second status word will be the status of the Receiving RT.

6.3.2.5 Time-Tag

The seventh location in the Monitor Block is the time-tag associated with the message. The time-tag is stored into this location at the end of message processing (i.e., captured after the command is validated).

6.3.2.6 Reserved

The last location in the Monitor Block is reserved.

6.3.3 Monitor Block Chaining

The host determines the first Monitor Block by setting the start address in the Initial Monitor Block Pointer Register. Figure 22 shows the Monitor Block as the blocks execute in a contiguous fashion.

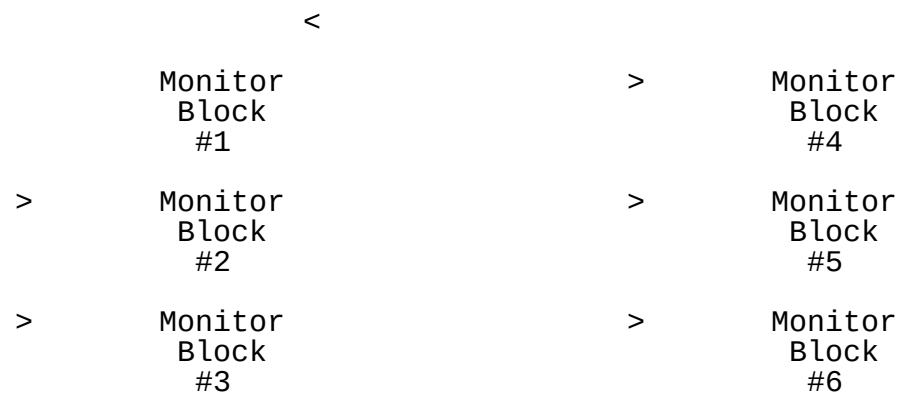


Figure 22. BM Monitor Block Structuring

6.3.4 Memory Architecture

The configuration shows the Monitor Blocks, data locations, and the Interrupt Log List as separate entities. Figure 23 shows that the first block of memory is allocated for the Monitor Blocks. Notice that Initial Monitor Block Pointer Register points to the initial Monitor Block location, Initial Monitor Data Pointer Register points to the initial Data location, Interrupt Log List Pointer Register points to the Interrupt Log, and Monitor Block Counter Register contains the Monitor Block count. After execution begins, the EXC-1553VME/MCH will build command blocks and store data words until the count reaches zero. When the count reaches zero, the EXC-1553VME/MCH will simply wrap back to the initial values and start again.

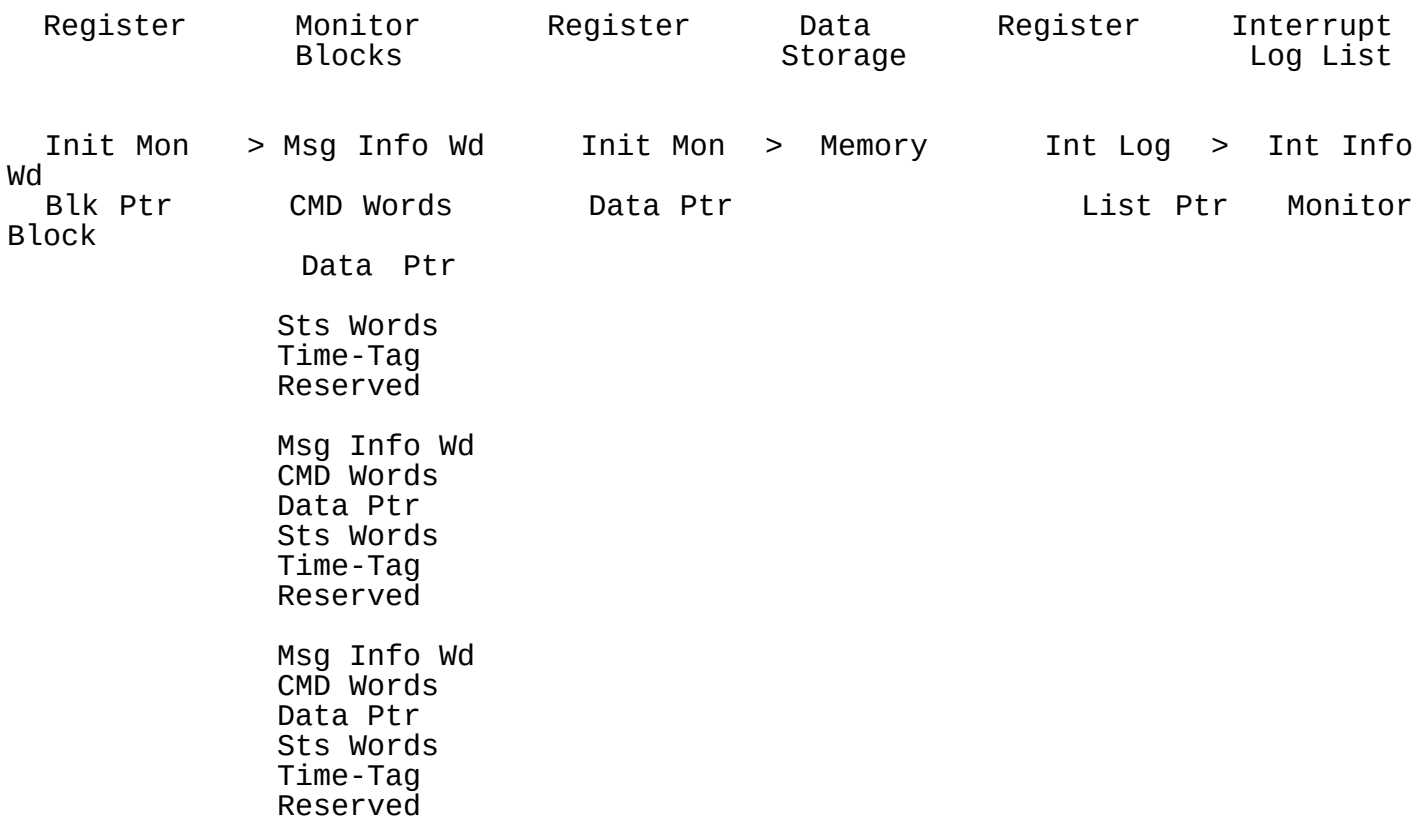


Figure 23. BM Memory Architecture

6.3.5 Message Processing

To process messages, the Bus Monitor uses data supplied in the control registers along with RAM memory. The Bus Monitor uses seven memory locations for each message called a monitor block. The monitor block is updated at the end of command processing. The following paragraphs discuss the command block in detail.

The user allocates memory spaces for each monitor block. The top of the monitor blocks can reside at any address location. Initialized by the host, the control registers are linked to the Monitor Block via the Initial Monitor Block Pointer Register and the Monitor Block Counter Register contents. Each monitor block contains a Message Information Word, Command Word 1, Command

Word 2, Data Pointer, Status Word 1, Status Word 2, and Time-Tag. Refer to section Bus Monitor Architecture for a full description of each location.

The Message Information word allows the EXC-1553VME/MCH to inform the user on which bus the command was received, whether the message was an RT-RT transfer, and conditions associated with the message. The EXC-1553VME/MCH also stores each command word associated with the message into the appropriate location. For normal 1553 commands, only the first command word location will contain data. For RT-RT commands, the second command word location will contain data, and bit 8 in the Message Information word will be set.

For each command, the Data Pointer determines where to store data words. The Bus Monitor stores data sequentially from the top memory location. The Bus Monitor also stores each status word associated with the message into the appropriate location. For normal 1553 commands, only the first status word location will contain data. For RT-RT commands, the second status word location will contain data.

The EXC-1553VME/MCH begins monitoring after Control Register bit 15 = 1 (i.e., assertion of TERACT and STEX). After reception, the EXC-1553VME/MCH begins post-processing. Command post-processing involves storing data to memory. An optional interrupt log entry is performed after a monitor is entered. Monitor Time-Out:

MIL-STD-1553A = 11 usec
MIL-STD-1553B = 15 usec

6.3.6 RT/ Concurrent BM Operation

For applications that require simultaneous Remote Terminal and Bus Monitor operations, the EXC-1553VME/MCH should be configured as both a remote terminal and monitor. This feature allows the RT to communicate on the bus for one specific address and the Bus Monitor to monitor the bus for other specific addresses. Configuration as both Bus Monitor and RT precludes the EXC-1553VME/MCH from monitoring its own remote terminal address.

When the EXC-1553VME/MCH is configured as both RT and Bus Monitor, the RT has priority over the Bus Monitor. For example, commands to the RT will always take priority over commands for the Bus Monitor. The examples below describe what happens if the RT is defined for terminal address 1 and the Bus Monitor is to monitor terminal address 12.

Example 1:

Bus A CMD (TA = 12)

Bus B CMD (TA = 1)

In this example, the Bus Monitor will decode the first command on bus A, realize the message is for terminal address 12, and start monitoring the message. However, as soon as the EXC-1553VME/MCH realizes the second command on bus B is to terminal address 1, the RT will take priority and begin RT message processing.

Example 2:

```
Bus A     CMD (TA = 1)

Bus B            CMD (TA = 12)
```

In example 2, the RT will decode the first command on bus A, realize the message is for terminal address 1, and start message processing. As the message on bus B is received, the EXC-1553VME/MCH will realize it is to terminal address 12. But, since the RT has priority, the Bus Monitor will not switch to the monitor mode.

The above examples also apply to an RT-RT message. For example, if the first command in an RT-RT transfer matches the terminal address of the RT, the entire message will be stored (Message 1). However, if the first command in an RT-RT transfer matches the terminal address of the Bus Monitor and the second command matches the terminal address of the RT, the RT will take priority and only the RT message is stored (Message 2). Below is an RT-RT message example.

```
Message 1     CMD (TA = 1)   CMD (TA = 12)

Message 2     CMD (TA = 12)  CMD (TA = 1)
```

6.3.7 MIL-STD-1553A Operation

The EXC-1553VME/MCH may be configured to meet the MIL-STD-1553A protocol.

A/B_STD	ERTO	RESULT
0	0	1553B standard, 1553B response (in 14 usec)
0	1	1553B standard, extended response (in 30 usec)
1	0	1553A standard, 1553A response (in 9 usec)
1	1	1553A standard, extended response (in 21 usec)

When configured as a MIL-STD-1553A monitor, the EXC-1553VME/MCH will operate as follows:

- looks for the RT response within 9 usec;
- ignores the T/R bit for all mode codes;
- defines all mode codes without data;
- defines subaddress 00000 as a mode code.

6.4 CHANNEL INTERRUPT ARCHITECTURE

The EXC-1553VME/MCH channel interrupt architecture involves three control registers, an Interrupt Log List, and the interrupt line. The three control registers include a Pending Interrupt Register, Interrupt Mask Register, and Interrupt Log List Register. The Pending Interrupt Register contains information that identifies the events generating the interrupts. The Interrupt Mask Register allows the user to mask or disable the generation of interrupts. The Interrupt Log List Register contains the base address of a 32-word interrupt ring buffer.

The lower twelve interrupt bits of the Pending Interrupt Register are entered into the Interrupt Log List, if the Interrupt Log List is enabled.

The interrupt architecture allows for the entry of 16 interrupts into a 32-word ring buffer (see figure 24). The EXC-1553VME/MCH channel automatically handles the interrupt logging overhead. Each interrupt generates two words of information to assist the host in performing interrupt processing. The interrupt Identification Word (IIW) identifies the type(s) of interrupt that occurred. The Interrupt Address Word (IAW) identifies the interrupt source (e.g., subaddress or command block) via a 16-bit address.

6.4.1 Interrupt Identification Word (IIW)

The Interrupt Identification Word (IIW) is a 16-bit word identifying the interrupt type. The format is similar to the Pending Interrupt Register. The host reads the IIW to determine which interrupt event occurred. The bit description for the IIW is provided below.

Bit	Name	Description
15-12	reserved	Set to '0'.
11	MERR	Message Error Interrupt (All modes).
10	SUBAD	Subaddress Accessed Interrupt (RT Mode).
9	BDRCV	Broadcast Command Received Interrupt (RT Mode).
8	IXEQ0	Index Equal Zero Interrupt (RT Mode).
7	ILCMD	Illegal Command Interrupt (RT Mode).
6	reserved	Set to '0'.
5	EOL	End of List (BC Mode).
4	ILLCMD	Illogical Command (BC Mode).
3	ILLOP	Illogical Opcode (BC Mode).
2	RTF	Retry Fail (BC Mode).
1	CBA	Command Block Accessed (BC Mode).
0	MBC	Monitor Block Count Equal Zero (BM Mode).

6.4.2 Interrupt Address Word (IAW)

The Interrupt Address Word (IAW) is a 16-bit word that identifies the interrupt source. Depending on the mode of operation (i.e., RT, BC, or BM), the IAW has different meanings. In the RT mode operation, the IAW identifies the subaddress or mode code descriptor that generated the interrupt. For the BC mode of operation, the IAW points to the command block addressed when the interrupt occurred. In the BM mode of operation, the IAW marks the monitor counter count when the interrupt occurred. The user uses the IAW with the Initial Monitor Command Block Pointer Register to determine the monitor command block that generates the interrupt.

When in RT/ Concurrent BM mode, the user must determine if the IAW contains information for the RT or BM. The determination is made by comparing the contents of the IAW base address with the descriptor base address. If a match occurs, then the IAW contains a subaddress or mode code identifier. If no match occurs, the IAW contains monitor counter information.

6.4.3 Interrupt Log List Address

The interrupt log list resides in a 32-word ring buffer. The host defines the location buffer, within the memory space, via the Interrupt Log List Register. Restrict the ring buffer address to a 32-word boundary.

During initialization the user writes a value to the Interrupt Log List Pointer Register. Initialize the least significant five-bits to a logic zero. The most significant 11 bits determine the base address of the buffer. The EXC-1553VME/MCH increments the ring buffer pointer on the occurrence of the first interrupt, storing the IIW and IAW at buffer locations 00H and 02H respectively. The EXC-1553VME/MCH logs ensuing interrupts sequentially into the ring buffer until interrupt number 16 occurs. The EXC-1553VME/MCH enters interrupt 16's IIW in buffer location 3CH and the IAW at location 3EH.

The EXC-1553VME/MCH increments the ring buffer pointer as interrupts occur. The least significant five-bits of the Interrupt Log List Pointer Register reflect the ring buffer pointer value. Figure 24 shows the ring buffer architecture.

The user reads the ring buffer pointer value to determine the number of interrupts that have occurred. By extracting the least significant five bits from the Interrupt Log List Register and logical shifting the data once to the right, the user determines the number of interrupt events.

Ring-Buffer Pointer

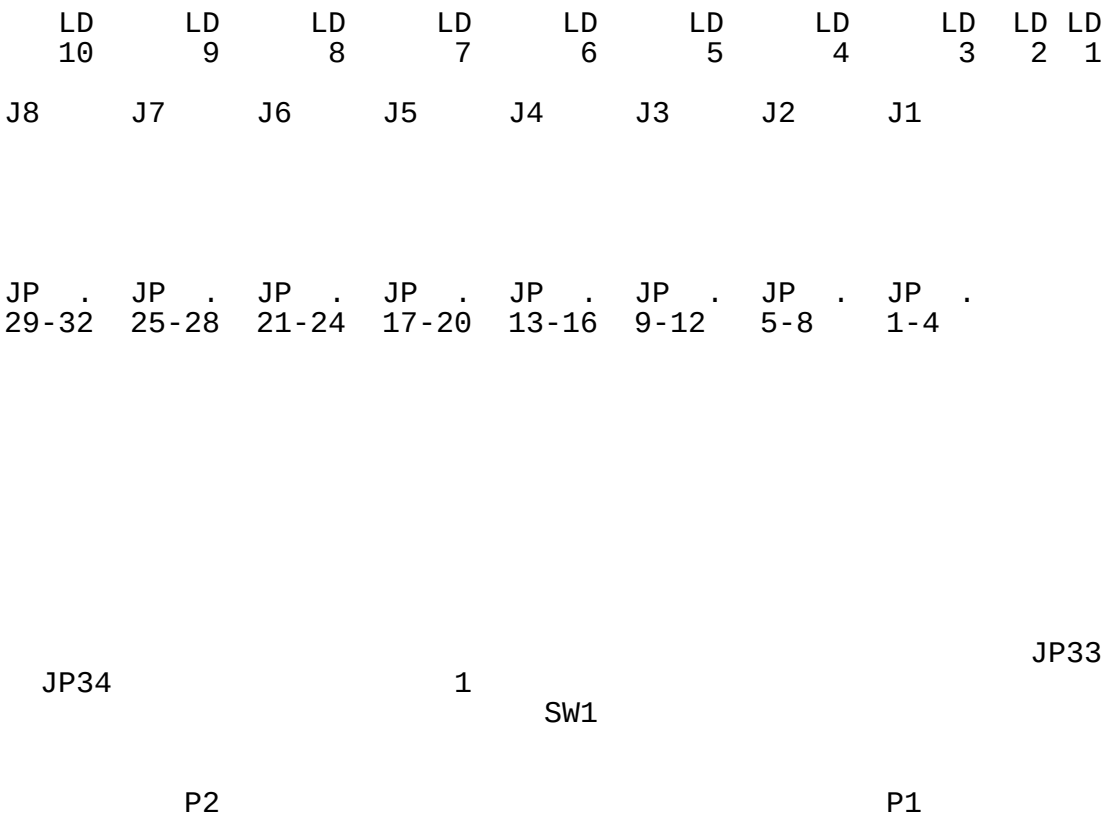
Base Address + 00 (H)	IIW #1	Base Address + 20 (H)	IIW #9
Base Address + 02 (H)	IAW #1	Base Address + 22 (H)	IAW #9
Base Address + 04 (H)	IIW #2	Base Address + 24 (H)	IIW #10
Base Address + 06 (H)	IAW #2	Base Address + 26 (H)	IAW #10
Base Address + 08 (H)	IIW #3	Base Address + 28 (H)	IIW #11
Base Address + 0A (H)	IAW #3	Base Address + 2A (H)	IAW #11
Base Address + 0C (H)	IIW #4	Base Address + 2C (H)	IIW #12
Base Address + 0E (H)	IAW #4	Base Address + 2E (H)	IAW #12
Base Address + 10 (H)	IIW #5	Base Address + 30 (H)	IIW #13
Base Address + 12 (H)	IAW #5	Base Address + 32 (H)	IAW #13
Base Address + 14 (H)	IIW #6	Base Address + 34 (H)	IIW #14
Base Address + 16 (H)	IAW #6	Base Address + 36 (H)	IAW #14
Base Address + 18 (H)	IIW #7	Base Address + 38 (H)	IIW #15
Base Address + 1A (H)	IAW #7	Base Address + 3A (H)	IAW #15
Base Address + 1C (H)	IIW #8	Base Address + 3C (H)	IIW #16
Base Address + 1E (H)	IAW #8	Base Address + 3E (H)	IAW #16

Interrupt Log List Address Register Contents

Interrupt Log List Address Register Contents

Figure 24. Interrupt Ring Buffer

7.0 BOARD LAYOUT



Note: B size card shown.

Figure 25. Board Layout

8.0 LEDS

The individual functions of the front panel leds are listed below.

MODID (LD1) Reflects the state of the MODID pin on the VXI bus (JP34 must be installed). This LED has no function in a VME system.

READY (LD2) Indicates that the card is ready to receive commands. Reflects the state of the bit of the same name in the Configuration Status Register.

CH #0 (LD3) Channel #0 Active. Indicates that a 1553 message is processed by the channel. Reflects the state of the TERACT bit in the channel #0 Operational Status Register.

CH #1 (LD4) Channel #1 Active. Indicates that a 1553 message is processed by the channel. Reflects the state of the TERACT bit in the channel #1 Operational Status Register.

CH #2 (LD5) Channel #2 Active. Indicates that a 1553 message is processed by the channel. Reflects the state of the TERACT bit in the channel #2 Operational Status Register.

CH #3 (LD6) Channel #3 Active. Indicates that a 1553 message is processed by the channel. Reflects the state of the TERACT bit in the channel #3 Operational Status Register.

CH #4 (LD7) Channel #4 Active. Indicates that a 1553 message is processed by the channel. Reflects the state of the TERACT bit in the channel #4 Operational Status Register.

CH #5 (LD8) Channel #5 Active. Indicates that a 1553 message is processed by the channel. Reflects the state of the TERACT bit in the channel #5 Operational Status Register.

CH #6 (LD9) Channel #6 Active. Indicates that a 1553 message is processed by the channel. Reflects the state of the TERACT bit in the channel #6 Operational Status Register.

CH #7 (LD10) Channel #7 Active. Indicates that a 1553 message is processed by the channel. Reflects the state of the TERACT bit in the channel #7 Operational Status Register.

9.0 DIP SWITCH SETTINGS

The EXC-1553VME/MCH board contains 1 Dip Switch which controls the Logical Address of board.

9.1 Card Logical Address Dip Switch Setting SW1

Dip switch SW1 is used to select the card's Logical Address as described in the section "VME/VXI Configuration Registers". The Logical Address is set as shown below.

Logical Address Switch (SW1)

```
            MSB                                   LSB

'1' '1'     1    2    3    4    5    6    7    8    -> numbers indicate
                                                       switch positions.
A15 A14    A13  A12  A11  A10   A9   A8   A7   A6

          Switch  "ON" or "Closed" =  logic 0 at bit position
          Switch  "OFF" or "OPEN"  =  logic 1 at bit position
```

Note: Address lines A15,A14 are always decoded as '1'.

Example: for a Logical Address of C0(H) (= A16 address F000H),
set positions '1'and '2' to "OFF" or "OPEN"
and ALL other positions to "ON" or "CLOSED".

9.2 Factory Default Dip Switch Settings

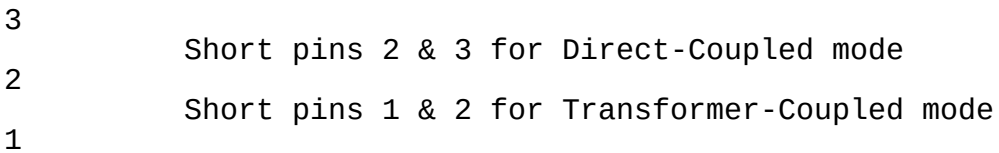
SW1 is set to Logical Address 80H (1 off; 2-8 on = A16 address E000 H)

10.0 JUMPERS

Groups of Jumper Headers are provided on the board for various user selectable functions. These headers are mounted with shorting blocks according to the default board setup (see Factory Default Jumper Settings section below). In high vibration environments these jumpers can be soldered or "Wire-Wrapped". Jumpers not appearing on the Board Layout are factory set and should not be used.

10.1 Channel #x 1553 Coupling Mode Select Jumpers [JP1-32]

Groups of four jumpers select the coupling mode to the channel #x 1553 bus. The EXC-1553VME/MCH can be either DIRECT or TRANSFORMER coupled to the 1553 bus.
Refer to this diagram for all 32 jumpers.



Channel	Jumper Group
channel #0	JP1 -JP4
channel #1	JP5 -JP8
channel #2	JP9 -JP12
channel #3	JP13-JP16
channel #4	JP17-JP20
channel #5	JP21-JP24
channel #6	JP25-JP28
channel #7	JP29-JP32

10.2 VME Address Space Select Jumper [JP33]

This jumper selects the VME Address Space that the board's memory will be located at.

Jumper shorted = A24 address space
Jumper open = A32 address space

10.3 VXI MODID Connect Jumper [JP34]

This jumper connects the card to the VXI 'MODID' signal located at P2-A30.

Jumper shorted = 'MODID' connected (ready for VXI environment)
Jumper open = 'MODID' disconnected (pin P2-A30 free for VME user-defined)

10.4 Factory Default Jumper Settings

The factory jumpers setup for VME is as follows:

JP1-JP32 set to Transformer-Coupled mode (pins 1 & 2 Shorted)
JP33 set to A24 Address Space (Shorted)
JP34 set to 'MODID' disconnected (Open)

The factory jumpers setup for VXI is as follows:

JP1-JP32 set to Transformer-Coupled mode (pins 1 & 2 Shorted)
JP33 set to A24 Address Space (Shorted)
JP34 set to 'MODID' connected (Shorted)

11.0 CONNECTORS

The EXC-1553VME/MCH contains ten connectors:

a) eight 6-pin Molex (micro-fit) connectors (J1 to J8), one per channel

b) two DIN type 96 pin VME/VXI connectors (P1 and P2)

11.1 Connector Jx Pinout

These 6 pin MOLEX 43045-0600 connectors contain all signals relevant to a specific channel. Mating connectors (43025-0600) with crimp terminals (43030) are included. Each connector is associated with a specific channel:

Channel	Connector
channel #0	J1
channel #1	J2
channel #2	J3
channel #3	J4
channel #4	J5
channel #5	J6
channel #6	J7
channel #7	J8

Connector Jx Layout and Pin Assignments
(Front View)

Pin	Signal Name	Pin	Signal Name
5	BUS_B_HI	6	BUS_B_LO
3	SHIELD(case)	4	SHIELD(case)
1	BUS_A_HI	2	BUS_A_LO

Table 6. Connector Jx Pinout

Signals description:

BUS_A_HI
BUS_A_LO - Channel x, Bus A, connection.

BUS_B_HI
BUS_B_LO - Channel x, Bus B, connection.

SHIELD(case) - Provided for 1553 cables shield connection. This signal is connected to the VME system's case trough the front panel.

11.2 Connector P1 Pinout

Pin #	Sig. Name	Pin #	Sig. Name	Pin #	Sig. Name
A1	D00	B1		C1	D08
A2	D01	B2		C2	D09
A3	D02	B3		C3	D10
A4	D03	B4	BG0IN*	C4	D11
A5	D04	B5	BG0OUT*	C5	D12
A6	D05	B6	BG1IN*	C6	D13
A7	D06	B7	BG1OUT*	C7	D14
A8	D07	B8	BG2IN*	C8	D15
A9	GND	B9	BG2OUT*	C9	GND
A10	SYSCLK	B10	BG3IN*	C10	
A11	GND	B11	BG3OUT*	C11	
A12	DS1*	B12		C12	SYSRESET*
A13	DS0*	B13		C13	LWORD*
A14	WRITE*	B14		C14	AM5
A15	GND	B15		C15	A23
A16	DTACK*	B16	AM0	C16	A22
A17	GND	B17	AM1	C17	A21
A18	AS*	B18	AM2	C18	A20
A19	GND	B19	AM3	C19	A19
A20	IACK*	B20	GND	C20	A18
A21	IACKIN*	B21		C21	A17
A22	IACKOUT*	B22		C22	A16
A23	AM4	B23	GND	C23	A15
A24	A07	B24	IRQ7*	C24	A14
A25	A06	B25	IRQ6*	C25	A13
A26	A05	B26	IRQ5*	C26	A12
A27	A04	B27	IRQ4*	C27	A11
A28	A03	B28	IRQ3*	C28	A10
A29	A02	B29	IRQ2*	C29	A09
A30	A01	B30	IRQ1*	C30	A08
A31	-12V(opt)	B31		C31	
A32	+5V	B32	+5V	C32	+5V

Table 7. Connector P1 Pinout

11.3 Connector P2 Pinout

Pin #	Sig. Name	Pin #	Sig. Name	Pin #	Sig. Name
A1		B1	+5V	C1	
A2		B2	GND	C2	
A3		B3		C3	
A4		B4	A24	C4	
A5		B5	A25	C5	
A6		B6	A26	C6	
A7		B7	A27	C7	
A8		B8	A28	C8	
A9		B9	A29	C9	
A10		B10	A30	C10	
A11		B11	A31	C11	
A12		B12	GND	C12	
A13		B13	+5V	C13	
A14		B14		C14	
A15		B15		C15	
A16		B16		C16	
A17		B17		C17	
A18		B18		C18	
A19		B19		C19	
A20		B20		C20	
A21		B21		C21	
A22		B22	GND	C22	
A23		B23		C23	
A24		B24		C24	
A25		B25		C25	
A26		B26		C26	
A27		B27		C27	
A28		B28		C28	
A29		B29		C29	
A30	MODID (x)	B30		C30	
A31		B31	GND	C31	
A32		B32	+5V	C32	

Table 8. Connector P2 Pinout

Notes: (x) - VXI signals (each of them is unconnected, unless the specific jumper is shorted. See Jumpers section)

12.0 POWER REQUIREMENTS

The board's maximum power supply requirements are defined below.

EXC-1553VME/MCH with no channels installed:

+5V @ 1.0 Amps

Each installed channel requires:

+5V @ 150mA (0% duty cycle: non-transmitting on 1553 bus)
+5V @ 395mA (25% duty cycle transmitting on 1553 bus)
+5V @ 595mA (50% duty cycle transmitting on 1553 bus)
+5V @ 895mA (80% duty cycle transmitting on 1553 bus)
+5V @ 895mA (100% duty cycle transmitting on 1553 bus)

Example:
8 channel board (@ 25% duty cycle per channel) maximum power requirements will be: +5V @ 4.16A (1.0A + 8 x 0.395A = 4.16A)

13.0 ORDERING INFORMATION

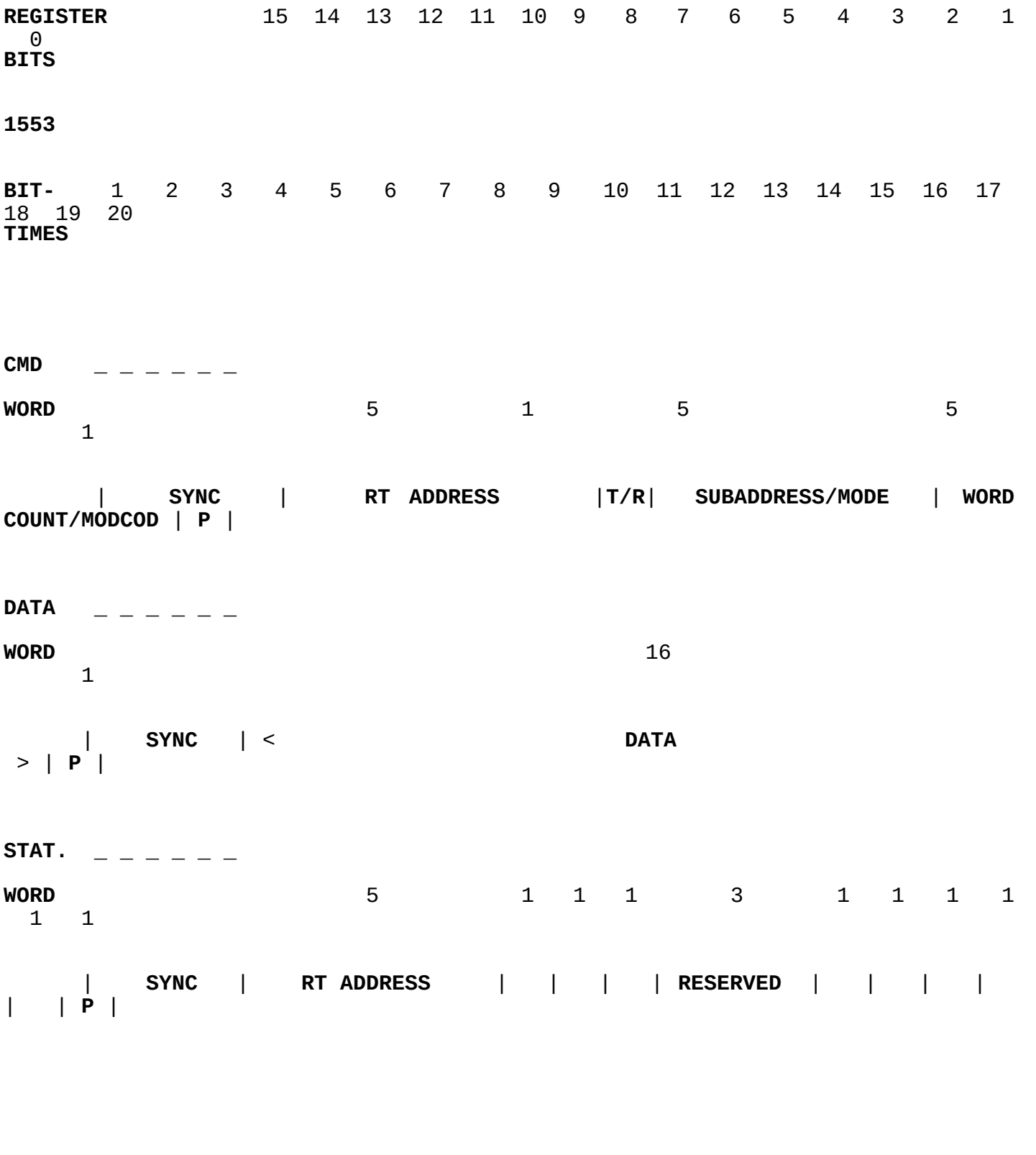
Part Number	Description	Note
EXC-1553VME/MCH-x	Multi-Channel 1553 VME/VXI B-size (6"x9") board. Supports BC, RT, RT/BM and BM Modes.	
EXC-1553VME/MCH-x-E	Same as above with Ruggedization and Extended Temperature (-40^{o} to $+85^{o}$ C) operation.	1
EXC-1553VXI/MCH-x	Multi-Channel 1553 VXI C-size (13"x9") board. Supports BC, RT, RT/BM and BM Modes. Supplied with RFI/EMI shield.	
EXC-1553VXI/MCH-x-E	Same as above with Ruggedization and Extended Temperature (-40^{o} to $+85^{o}$ C) operation.	1
	x = number of channels required (up to 8)	
EXC-1553UPG/MCH	Additional Channel upgrade.	2

Note: 1) Products with '-E' suffix come with a board stiffener and all components are soldered onto the printed circuit board (sockets are not used), enabling use in high vibration environments.

2) Factory installed upgrades for additional channels (to a maximum of 8) may be ordered.

APPENDIXES

APPENDIX A: MIL-STD-1553B WORD FORMATS


REGISTER 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
BITS
1553
BIT- 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
TIMES
CMD _ _ _ _ _ _
WORD 5 1 5 5 1
| SYNC | RT ADDRESS |T/R| SUBADDRESS/MODE | WORD COUNT/MODCOD | P |
DATA _ _ _ _ _ _
WORD 16 1
| SYNC | < DATA > | P |
STAT. _ _ _ _ _ _
WORD 5 1 1 1 3 1 1 1 1 1 1
| SYNC | RT ADDRESS | | | | RESERVED | | | | | P |

Appendix A

MESSAGE ERROR

INSTRUMENTATION

SERVICE REQUEST

BROADCADST COMMAND RCV'D

BUSY

SUBSYSTEM FLAG

DYNAMIC BUS CONTROL ACCEPTANCE

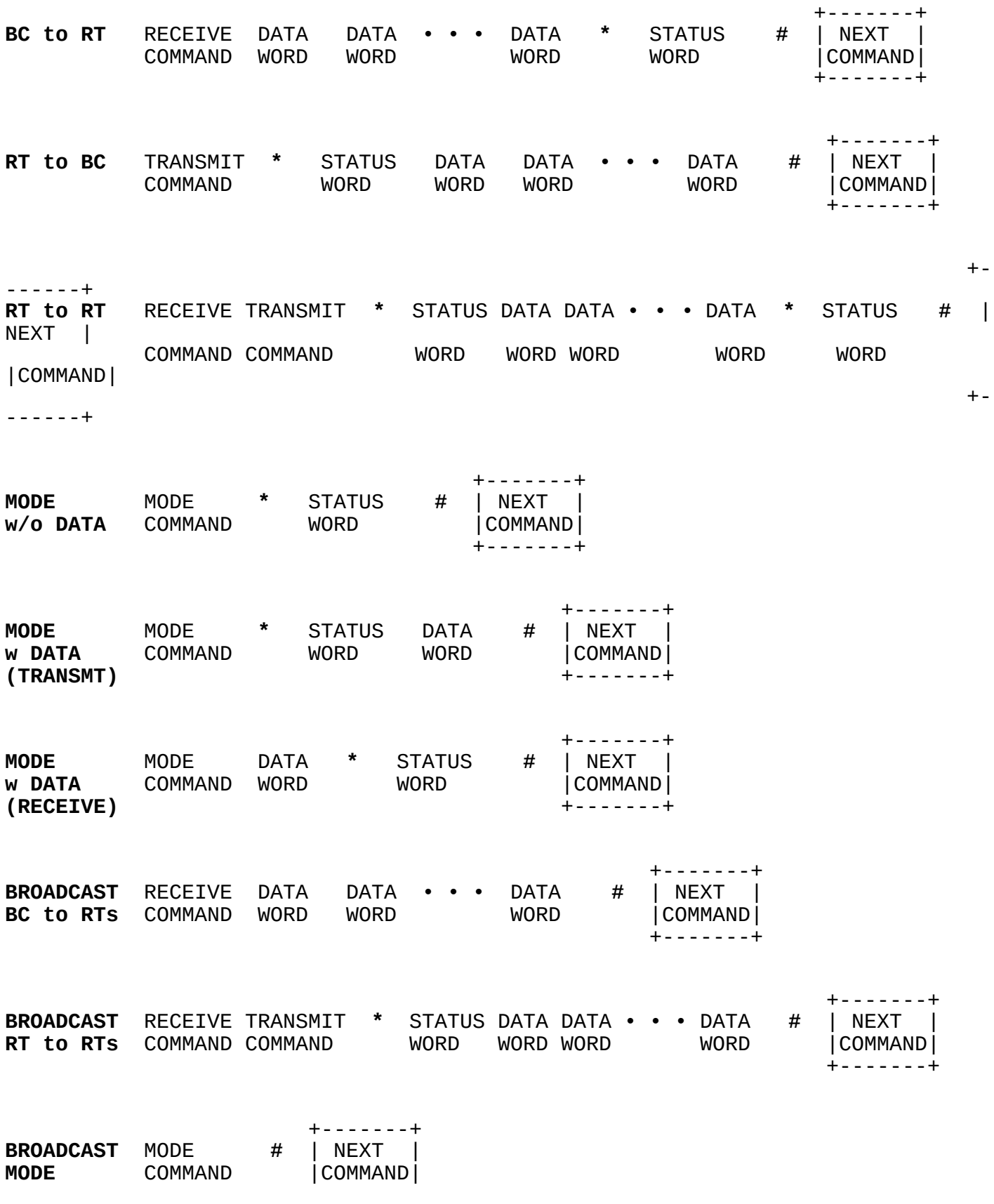
TERMINAL

FLAG

Note:
T/R - transmit/receive
MODCOD - mode code
P - parity

Figure 26. MIL-STD-1553B Word Formats

APPENDIX B: MIL-STD-1553B MESSAGE FORMATS



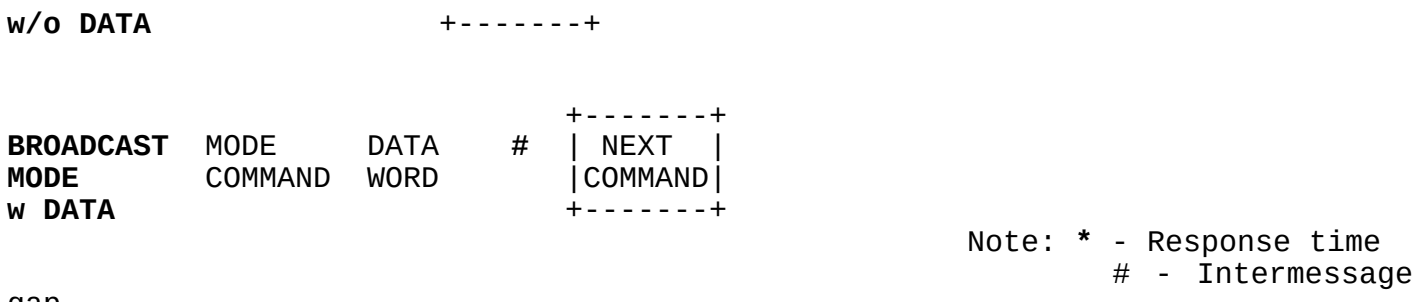


Figure 27. MIL-STD-1553B Message Formats

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